xCORE VocalFusion Speaker Evaluation Kit Hardware Manual

IN THIS DOCUMENT

The **xCORE VocalFusion Speaker Evaluation Kit** is an application specific design for far-field voice capture and processing, targeted at voice user interfaces (VUI) for home and conferencing applications.

The kit is based on the XVF3100 voice processor and includes:

- linear or circular array of 4 omni-directional microphones:
  - circular: 360° capture, for 'centre of the room' applications
  - linear: up to 180° capture, for 'edge of the room' applications
- low-jitter audio clock
- configurable user input buttons and LEDs
- host connectivity as USB2.0 device and/or I2S and I2C
- USB powered

Publication Date: 2018/8/15

Document Number: XM010448A

When loaded with VocalFusion software, the XVF3100 on the kit implements the xCORE VocalFusion[1] microphone capture and voice processing library, audio and control connectivity, user interfaces and system control.

Developers who wish to use their own microphone and voice DSP libraries should use the xCORE Microphone Array board[2] based on a fully featured two-tile xCORE-200 XUF216-512-TQ128 device.

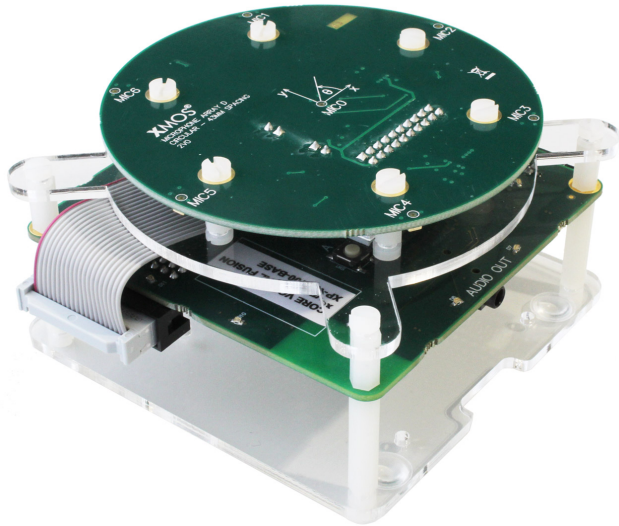

Figure 1: xCORE VocalFusion Speaker circular kit

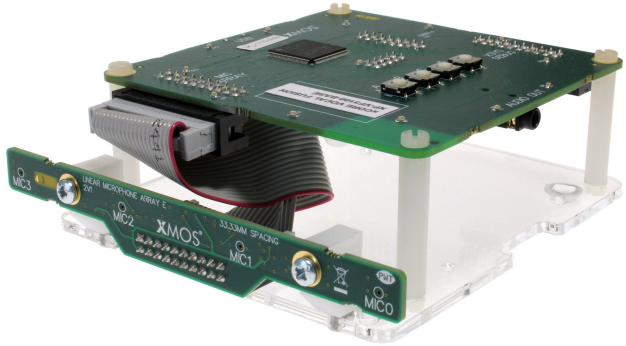

Figure 2: xCORE VocalFusion Speaker linear kit

[1] http://www.xmos.com/vocalfusion
[2] http://www.xmos.com/usbarraymic

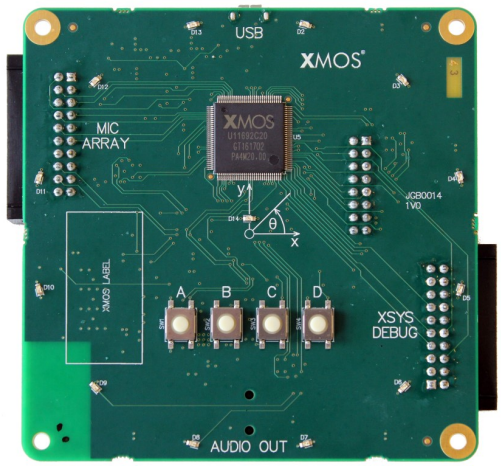

Figure 3: xCORE VocalFusion BaseBoard

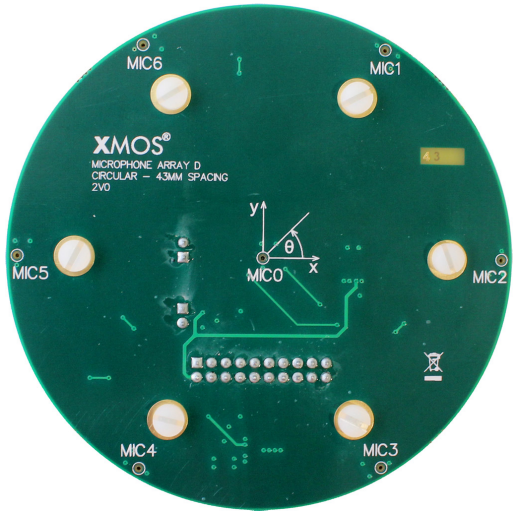

Figure 4: xCORE VocalFusion Circular Microphone board

Figure 5: xCORE VocalFusion Linear Microphone board

1 Features

The **xCORE VocalFusion Speaker Evaluation Kit** block diagram is shown in Figure 6 below. It includes:

- xCORE VocalFusion XVF3100 Voice Processor
- Four MEMS microphones on a separate board
- A micro-USB connector for USB2.0 device connectivity and power
- An extension header for I2S, I2C and/or other connectivity and control solutions
- Four general purpose push-button switches
- 13 user-controlled LEDs
- Low-jitter clock source
- An xSYS connector for an xTAG debug adapter

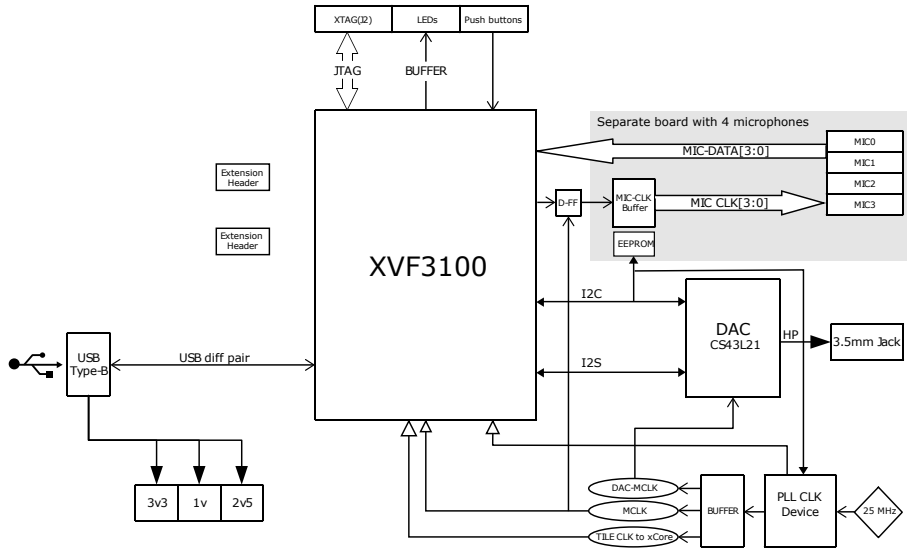

Figure 6: xCORE VocalFusion Speaker Evaluation Kit block diagram

2 Introduction

The **xCORE VocalFusion Speaker Evaluation Kit** consists of an xCORE VocalFusion BaseBoard and separate MEMS microphone board, enabling the use of different microphone configurations. The evaluation kit is available with a circular microphone array (XK-VF3100-C43, Figure 1) and the other with a linear microphone array (XK-VF3100-L33, Figure 2).

Both the circular microphone board and the linear microphone board use Infineon IM69D130[3] MEMS microphones.

This document refers to kits with version 1V0 of the linear array and 2V0 of the circular array. For details on previous versions, please refer to the product page on the XMOS website[4].

The VocalFusion BaseBoard is based on the XVF3100 device, running a software which integrates the xCORE VocalFusion microphone capture and voice processing library providing: beamforming, Acoustic Echo Cancellation (AEC), noise suppression, de-reverberation and Automatic Gain Control (AGC).

The XVF3100 device has 16 32-bit logical processing cores and integrates 2MBytes Quad Serial Peripheral Interface (QSPI) flash in a TQ128 package.

Developers who wish to use their own microphone and acoustic DSP libraries should use the xCORE Microphone Array board[5] based on a fully featured two-tile xCORE-200 XUF216-512-TQ128 device.

For device specific information on the XVF3100 device see the XVF3100 Datasheet[6]. For general information on XVF and xCORE-200 devices see the xCORE-200 Architecture Overview[7].

[3] http://www.infineon.com/microphones
[4] http://www.xmos.com/support/boards-selector
[5] http://www.xmos.com/usbarraymic
[6] http://www.xmos.com/published/xvf3000_3100-tq128-datasheet
[7] http://www.xmos.com/published/xcore-architecture

3 Clock sources and distribution

The board includes a single clock generator (Si5351A-B04486-GT, U25) that generates two clocks:

- XVF3100 reference clock - 24MHz oscillator
- Low jitter master clock - 24.576MHz oscillator, used for the DAC and (indirectly) the microphones

The clock generator is controlled by the XVF3100 over the I2C bus (see Figure 7 below).

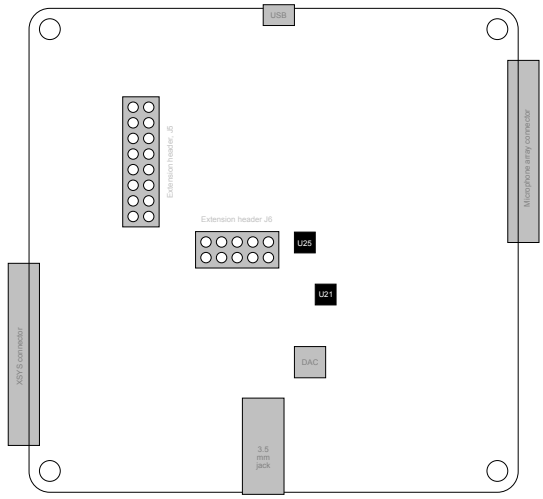

Figure 7: Clock generator and buffer locations

4 Stereo DAC with headphone amplifier

A CS43L21 stereo DAC with integrated headphone amplifier is used to generate audio output on a 3.5mm audio jack. The CS43L21 is connected to the XVF3100 device through an I2S interface and is configured using the I2C bus (see Figure 7 below). The DAC can operate as I2S master (XVF3100 is slave) or slave (XVF3100 is master).

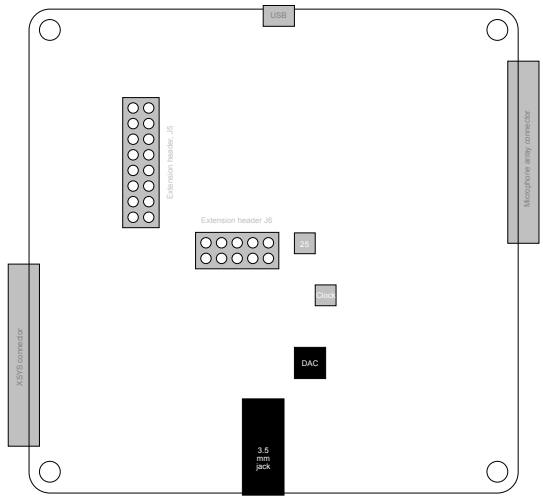

Figure 8: DAC and 3.5mm audio jack locations

The I2S interface of the CS43L21 stereo DAC/HPA device is connected to the XVF3100 GPIO pins as shown in Figure 9 below.

Pin	Port	Signal
X1D28	P4F0	DAC_RST_N
X1D36	P1M0	I2S_BCLK
X1D37	P1N0	I2S_LRCK
X1D38	P1O0	MCLK_TILE1
X1D39	P1P0	I2S_DAC_DATA

Figure 9: Stereo DAC GPIO pins

5 MEMS Microphone boards

The microphone board is plugged into connector J3 on the BaseBoard using a ribbon cable (see Figure 10). A short ribbon cable should be used for signal integrity.

The microphones should **not** be plugged into the xSYS connector.

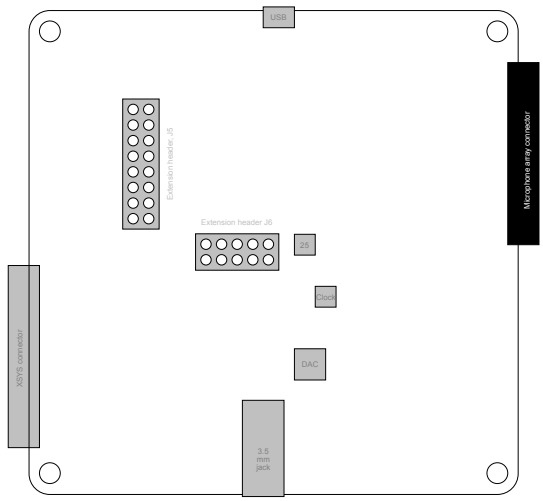

Figure 10: Microphone connector location

Two different microphone configurations are available with VocalFusion Speaker Evaluation Kit:

- Linear microphone array board (see Figure 5)

  The linear microphone board array consists of a linear array of four microphones, spaced 33.33mm apart, a clock buffer, and an EEPROM for optional identification.

  The microphone signals are mapped onto the XVF3100 device as show in Figure 11.

- Circular microphone array board (see Figure 4)

  The circular microphone board has 7 microphones of which the software uses four: microphones 1,3,4 and 6. These four microphones are on the corners of a rectangle of 43mm on the short side and 74.5mm on the long side.

  The board also includes a clock buffer, and an EEPROM for optional identification.

  The microphone signals are mapped onto the XVF3100 device as show in Figure 12. This enables up to eight microphones to be connected.

Other microphone configurations can be supported as detailed in the software manual.

Microphone	GPIO pin	Port
MIC_CLK	X0D12	P1E0
MCLK_IN	X0D13	P1F0
MIC_0	X0D14	P8B0
MIC_1	X0D15	P8B1
MIC_2	X0D16	P8B2
MIC_3	X0D17	P8B3

Figure 11: Linear MEMS microphone board GPIO pins

Microphone	GPIO pin	Port
MIC_CLK	X0D12	P1E0
MCLK_IN	X0D13	P1F0
MIC_1	X0D15	P8B1
MIC_3	X0D17	P8B3
MIC_4	X0D18	P8B4
MIC_6	X0D20	P8B6

Figure 12: Circular MEMS microphone board GPIO pins

6 I2C bus

The BaseBoard has a main I2C bus that is used to control the DAC, clock generator, and any EEPROM. This main I2C bus is connected to tile 1 of the XVF3100, with the XVF3100 acting as a master on the I2C bus. See Figure 13 below.

Pin	Port	Signal
X1D26	P4E0	I2C_SCL
X1D27	P4E1	I2C_SDA

Figure 13: I2C master GPIO pins

The addresses of devices on the I2C bus are shown in Figure 14 below.

Device	Address	
Si5351A (Clock)	0b1100010	0x62
CS43L21 (DAC)	0b1001010	0x4A
24LC08B (EEPROM on microphone board)	0b1010Xxx	0x5x

Figure 14: I2C master GPIO pins

Please refer to the 24LC08B datasheet for details on how to address of the EEPROM.

The BaseBoard also has an (optional) secondary I2C bus, on which the XVF3100 is a slave so allowing the XVF3100 to be controlled by an external I2C host. See Figure 15 below.

Figure 15: I2C slave GPIO pins

GPIO pin	Port	Signal
X0D24	P1I0	I2C_SDA_SLAVE
X0D25	P1J1	I2C_SCL_SLAVE

This slave I2C interface is wired up to the extension headers (see §8).

Pull-up resistors of 4.7kΩ are installed.

7 General purpose user interface

The BaseBoard has 13 LEDs that are controlled by the XVF3100 GPIO. LED_0 - LED_11 (D2-D13) are positioned around the edge of the BaseBoard. LED_12 (D14) is positioned in the middle of the BaseBoard.

The LED output must be set low to light the corresponding LED.

Four general purpose push-button switches are provided. When pressed, each button creates a connection from the I/O to GND. To ensure correct behavior, the port connected to the buttons (P4A) must always be defined as an input.

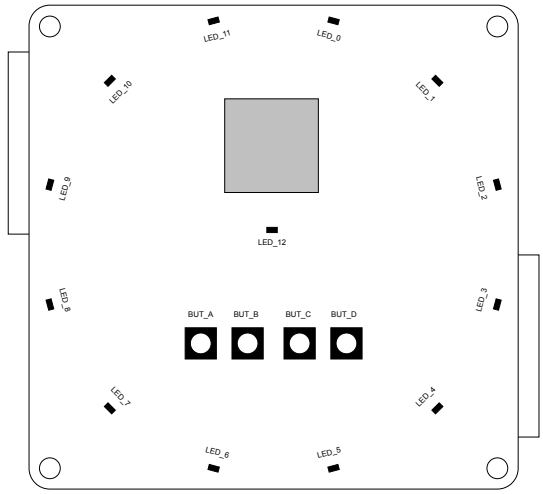

Figure 16: General purpose user interface components

The signal mapping of the user interface components to the XVF3100 GPIO is shown in Figure 17 and Figure 18

UI signal	GPIO pin	Port
BUTTON_A	X0D02	P4A0
BUTTON_B	X0D03	P4A1
BUTTON_C	X0D08	P4A2
BUTTON_D	X0D09	P4A3

Figure 17: User interface GPIO

A green LED (PGOOD) near the USB connector indicates 3V3 and 1V0 supplies are up.

UI signal	GPIO pin	Port
LED_0	X0D26	P16B0
LED_1	X0D27	P16B1
LED_2	X0D28	P16B2
LED_3	X0D29	P16B3
LED_4	X0D30	P16B4
LED_5	X0D31	P16B5
LED_6	X0D32	P16B6
LED_7	X0D33	P16B7
LED_8	X0D34	P1K0
LED_9	X0D35	P1L0
LED_10	X0D36	P16B8
LED_11	X0D37	P16B9
LED_12	X0D38	P16B10

Figure 18: User interface GPIO

8 Extension Headers

The BaseBoard has a two extension headers, J5 and J6, containing digital audio signals, the secondary I2C bus (see §6) and several general purpose IOs controlled by the XVF3100.

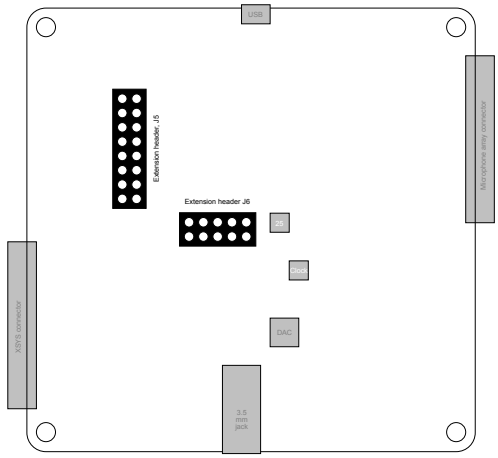

Figure 19: Extension header location

The BaseBoard supports a variety of methods to communicate audio and control data between the XVF3100 and a host applications processor; such as: USB, I2S and/or I2C.

The audio and control connectivity is defined by the software running on the XVF3100. This software also defines the functionality of the extension headers.

The xCORE VocalFusion Speaker Evaluation Kit as supplied is not flashed with software. To load an existing software see the Quick Start Guide[8]. To build and load a software see the Getting Started Guide[9].

Below are extension header configurations for three example softwares.

XVF3100 as a USB 2.0 device

- Example VocalFusion build configuration: `1i2o2_cir43_usbctl`
- Audio input/output via USB. The XVF3100 is a USB Audio Class 1 device.
- Control via USB. The XVF3100 can be controlled as a custom vendor request control device.
- When using this mode, the extension headers are not used and should be left unconnected. For completeness the mapping of the XVF3100 GPIO to the extension headers is detailed in Figure 20 and Figure 21 below.

[8] http://www.xmos.com/published/xcore-vocalfusion-speaker-evaluation-kit-quick-start-guide
[9] http://www.xmos.com/published/sw_vocalfusion-sw_vocalfusion-getting-started-guide

J5 pin	GPIO pin	Port	Signal	Notes
1	X0D22	P1G0		*Not used*
2			GND	Ground
3	X0D23	P1H0		*Not used*
4	X1D35	P1L0		*Not used*
5	X0D00	P1A0		*Not used*
6			GND	Ground
7	X0D11	P1D0		*Not used*
8			GND	Ground
9	X0D24	P1I0	I2C_SDA_SLAVE	*Not used*
10	X0D39	P1P0		*Not used*
11			GND	Ground
12	X0D25	P1J0	I2C_SCL_SLAVE	*Not used*
13			3V3	3.3V from BaseBoard
14			GND	Ground
15			EXT_MCLK	MCLK input (not used)
16			GND	Ground

Figure 20: Extension header J5 GPIO pins (XVF3100 as a USB device)

J6 pin	GPIO pin	Port	Signal	Notes
1	X1D37	P1N0	I2S_LRCK	I2S LRCLK from XVF3100 to DAC
2			GND	Ground
3	X1D39	P1P0	I2S_DAC_DATA	I2S data from XVF3100 to DAC
4			NC	*No connection*
5			GND	Ground
6	X1D36	P1M0	I2S_BCLK	I2S BLCK from XVF3100 to DAC
7	X1D38	P1O0	MCLK_TILE1	I2S MCLK to XVF3100
8			GND	Ground
9	X1D11	P1D0	X1D11	*Not used*
10	X1D10	P1C0	X1D10	*Not used*

Figure 21: Extension header J6 GPIO pins (XVF3100 as a USB device)

XVF3100 as the I2S master

- Example VocalFusion build configuration: `1i0o0_lin33_i2s_only_master_48khz_i2cctl`
- Audio input/output via I2S signals on J6. The XVF3100 is the I2S master.
- Control via I2C on J5. The XVF3100 is an I2C slave. For maps
- Extension headers are mapped to the XVF3100 GPIO as shown in Figure 22 and Figure 23 below.

J5 pin	GPIO pin	Port	Signal	Notes
1	X0D22	P1G0		*Not used*
2			GND	Ground
3	X0D23	P1H0		*Not used*
4	X1D35	P1L0		*Not used*
5	X0D00	P1A0		*Not used*
6			GND	Ground
7	X0D11	P1D0		*Not used*
8			GND	Ground
9	X0D24	P1I0	I2C_SDA_SLAVE	Add a pull-up resistor
10	X0D39	P1P0		*Not used*
11			GND	Ground
12	X0D25	P1J0	I2C_SCL_SLAVE	Add a pull-up resistor
13			3V3	3.3V from BaseBoard
14			GND	Ground
15			EXT_MCLK	MCLK input (not used)
16			GND	Ground

Figure 22: Extension header J5 GPIO pins (XVF3100 as the I2S master)

J6 pin	GPIO pin	Port	Signal	Notes
1	X1D37	P1N0	I2S_LRCK	I2S LRCLK from XVF3100 to host (and DAC)
2			GND	Ground
3	X1D39	P1P0	I2S_DAC_DATA	I2S data from host to XVF3100 (and DAC)
4			NC	*No connection*
5			GND	Ground
6	X1D36	P1M0	I2S_BCLK	I2S BLCK from XVF3100 to host (and DAC)
7	X1D38	P1O0	MCLK_TILE1	MCLK output to host (and XVF3100)
8			GND	Ground
9	X1D11	P1D0	X1D11	I2S data from XVF3100 to host
10	X1D10	P1C0	X1D10	*Not used*

Figure 23: Extension header J6 GPIO pins (XVF3100 the I2S master)

XVF3100 as an I2S slave

To use this mode, remove R67 and insert a 0R link into R17.

- Example VocalFusion build configuration: `1i0o0_lin33_i2s_only_48kHz_i2cctl`
- Audio input/output via I2S on J6. The XVF3100 is an I2S slave.
- Control via I2C on J5. The XVF3100 is an I2C slave.
- 24.576 MHz MasterClock generated externally and connected to J5 pin 15.
- Extension headers mapped to the XVF3100 GPIO as shown in Figure 24 and Figure 25 below.

J5 pin	GPIO pin	Port	Signal	Notes
1	X0D22	P1G0		*Not used*
2			GND	Ground
3	X0D23	P1H0		*Not used*
4	X1D35	P1L0		*Not used*
5	X0D00	P1A0		*Not used*
6			GND	Ground
7	X0D11	P1D0		*Not used*
8			GND	Ground
9	X0D24	P1I0	I2C_SDA_SLAVE	Add a pull-up resistor
10	X0D39	P1P0		*Not used*
11			GND	Ground
12	X0D25	P1J0	I2C_SCL_SLAVE	Add a pull-up resistor
13			3V3	3.3V from BaseBoard
14			GND	Ground
15			EXT_MCLK	MCLK input from host to XVF3100 (and DAC)
16			GND	Ground

Figure 24: Extension header J5 GPIO pins (XVF3100 an I2S slave)

J6 pin	GPIO pins	Port	Signal	Notes
1	X1D37	P1N0	I2S_LRCK	I2S LRCLK from host to XVF3100 (and DAC)
2			GND	Ground
3	X1D39	P1P0	I2S_DAC_DATA	I2S data from host to DAC
4			NC	*No connection*
5			GND	Ground
6	X1D36	P1M0	I2S_BCLK	I2S BLCK from host to XVF3100 (and DAC)
7	X1D38	P1O0	MCLK_TILE1	MCLK output (not used)
8			GND	Ground
9	X1D11	P1D0	X1D11	I2S data from XVF3100 to host
10	X1D10	P1C0	X1D10	I2S data from host to XVF3100

Figure 25: Extension header J6 GPIO pins (XVF3100 as an I2S slave)

9 USB Port

The USB micro-B port (J1) is connected to the USB PHY integrated in the XVF3100 and provides USB interface connectivity.

The USB port also provides power for all the on-board circuits and is used to generate the following voltage rails:

- +1V0 (Core voltage to XMOS device)
- +2V5 (for headphone amplifier in DAC device)
- +3V3 for GPIOs and other accessory devices

Voltage tolerance should be as per USB VBUS specification values.

Proper power-on sequence is indicated by power good LED (D1) in bottom side of the board.

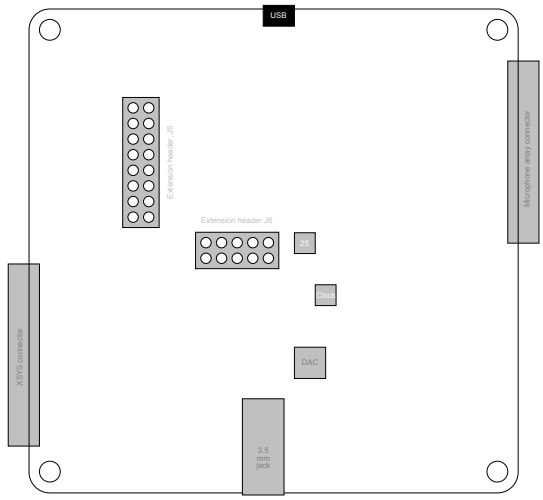

Figure 26: USB components

NOTE: J1 must be connected at all times to provide power to the board, even if the USB interface is not used.

10 Flash Memory

The XVF3100 device includes 2MBytes of QSPI flash memory, which is interfaced by the GPIO connections shown in Figure 27, below.

Figure 27: QSPI Flash GPIO pins

QSPI signal	GPIO pin	Port
QSPI_SS	X0D01	P1B
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C

11 xSYS connector

A standard XMOS xSYS interface (J2) is provided (Figure 28). This can connect to an XMOS xTAG debug adaptor, to allowing host debug of the board via JTAG.

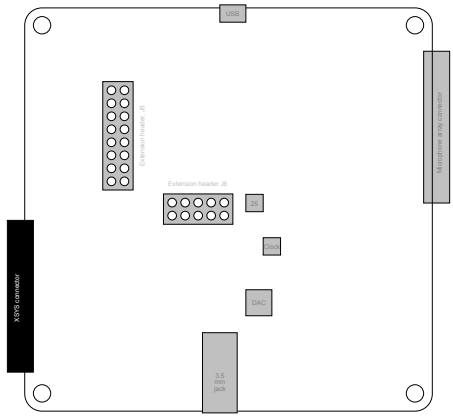

Figure 28: XSYS connector

xSYS signal	GPIO pin	Header pin	Description
TMS	See note	7	JTAG Test Mode Select
TCK	See note	9	JTAG Test Clock
TDI	See note	5	JTAG Test Data In - from debug adapter to xCORE
TDO	See note	13	JTAG Test Data Out - from xCORE to debug adapter
RST_N	See note	15	System Reset - active low, resets xCORE device
GND		4, 8, 12, 16, 20	Ground
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN0	X0D40	14	XMOS link, downlink bit 0
XL_DN1	X0D41	18	XMOS link, downlink bit 1

Figure 29: xSYS Connector Pinout

Notes:

- JTAG connections occupy dedicated connections

12 xCORE VocalFusion BaseBoard portmap

The tables below detail the port-pin mappings for the xCORE VocalFusion BaseBoard, as programmed with USB connectivity software.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	$1A^0$					
X0D01	$1B^0$					QSPI_CS
X0D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	BUTTON_A
X0D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	BUTTON_B
X0D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	QSPI_D0
X0D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	QSPI_D1
X0D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	QSPI_D2
X0D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	QSPI_D3
X0D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	BUTTON_C
X0D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	BUTTON_D
X0D10	$1C^0$					QSPI_CLK
X0D11	$1D^0$					
X0D12	$1E^0$					MIC_CLK
X0D13	$1F^0$					MCLK_IN
X0D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	MIC_0
X0D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	MIC_1
X0D16		$4D^0$	$8B^2$	$16A^{10}$		MIC_2
X0D17		$4D^1$	$8B^3$	$16A^{11}$		MIC_3
X0D18		$4D^2$	$8B^4$	$16A^{12}$		MIC_4
X0D19		$4D^3$	$8B^5$	$16A^{13}$		MIC_5
X0D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	MIC_6
X0D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	MIC_7
X0D22	$1G^0$					
X0D23	$1H^0$					
X0D24	$1I^0$					I2C_SDA_SLAVE
X0D25	$1J^0$					I2C_SCL_SLAVE
X0D26		$4E^0$	$8C^0$	$16B^0$		LED_0
X0D27		$4E^1$	$8C^1$	$16B^1$		LED_1
X0D28		$4F^0$	$8C^2$	$16B^2$		LED_2
X0D29		$4F^1$	$8C^3$	$16B^3$		LED_3
X0D30		$4F^2$	$8C^4$	$16B^4$		LED_4
X0D31		$4F^3$	$8C^5$	$16B^5$		LED_5
X0D32		$4E^2$	$8C^6$	$16B^6$		LED_6
X0D33		$4E^3$	$8C^7$	$16B^7$		LED_7
X0D34	$1K^0$					LED_8
X0D35	$1L^0$					LED_9
X0D36	$1M^0$		$8D^0$	$16B^8$		LED_10
X0D37	$1N^0$		$8D^1$	$16B^9$		LED_11
X0D38	$1O^0$		$8D^2$	$16B^{10}$		LED_12
X0D39	$1P^0$		$8D^3$	$16B^{11}$		
X0D40			$8D^4$	$16B^{12}$		XL_DN1
X0D41			$8D^5$	$16B^{13}$		XL_DN0
X0D42			$8D^6$	$16B^{14}$		XL_UP0
X0D43			$8D^7$	$16B^{15}$		XL_UP1

Figure 30: xCORE VocalFusion BaseBoard Portmap: Tile0

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X1D00	$1A^0$					
X1D01	$1B^0$					
X1D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	
X1D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	
X1D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	
X1D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	
X1D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	
X1D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	
X1D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	
X1D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	
X1D10	$1C^0$					I2S_ADC_DATA (not used)
X1D11	$1D^0$					
X1D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	
X1D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	
X1D16		$4D^0$	$8B^2$	$16A^{10}$		
X1D17		$4D^1$	$8B^3$	$16A^{11}$		
X1D18		$4D^2$	$8B^4$	$16A^{12}$		
X1D19		$4D^3$	$8B^5$	$16A^{13}$		
X1D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	
X1D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	
X1D26		$4E^0$	$8C^0$	$16B^0$		I2C_SCL
X1D27		$4E^1$	$8C^1$	$16B^1$		I2C_SDA
X1D28		$4F^0$	$8C^2$	$16B^2$		DAC_RST_N
X1D29		$4F^1$	$8C^3$	$16B^3$		
X1D30		$4F^2$	$8C^4$	$16B^4$		
X1D31		$4F^3$	$8C^5$	$16B^5$		
X1D32		$4E^2$	$8C^6$	$16B^6$		
X1D33		$4E^3$	$8C^7$	$16B^7$		
X1D35	$1L^0$					
X1D36	$1M^0$		$8D^0$	$16B^8$		I2S_BCLK
X1D37	$1N^0$		$8D^1$	$16B^9$		I2S_LRCK
X1D38	$1O^0$		$8D^2$	$16B^{10}$		MCLK_TILE1
X1D39	$1P^0$		$8D^3$	$16B^{11}$		*I2S_DAC_DATA**
X1D40			$8D^4$	$16B^{12}$		
X1D41			$8D^5$	$16B^{13}$		
X1D42			$8D^6$	$16B^{14}$		
X1D43			$8D^7$	$16B^{15}$		

Figure 31: xCORE VocalFusion BaseBoard Portmap: Tile1

13 Operating requirements

A USB 2.0 high-speed compliant cable should be used when operating the **xCORE VocalFusion Speaker Evaluation Kit**.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the xCORE VocalFusion Speaker Evaluation Kit with appropriate ESD precautions in place.

14 Dimensions

The xCORE VocalFusion BaseBoard is 90x90mm square and board thickness of 1.6mm.

15 RoHS and REACH

The xCORE VocalFusion Speaker Evaluation Kit complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The xCORE VocalFusion Speaker Evaluation Kit is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.

16 Schematics

The schematics for the BaseBoard included in the kit, are shown in the first five figures below, followed by the schematics for the linear and circular array board.

For full reference schematics please contact XMOS:

- https://www.xmos.com/contact/enquiries

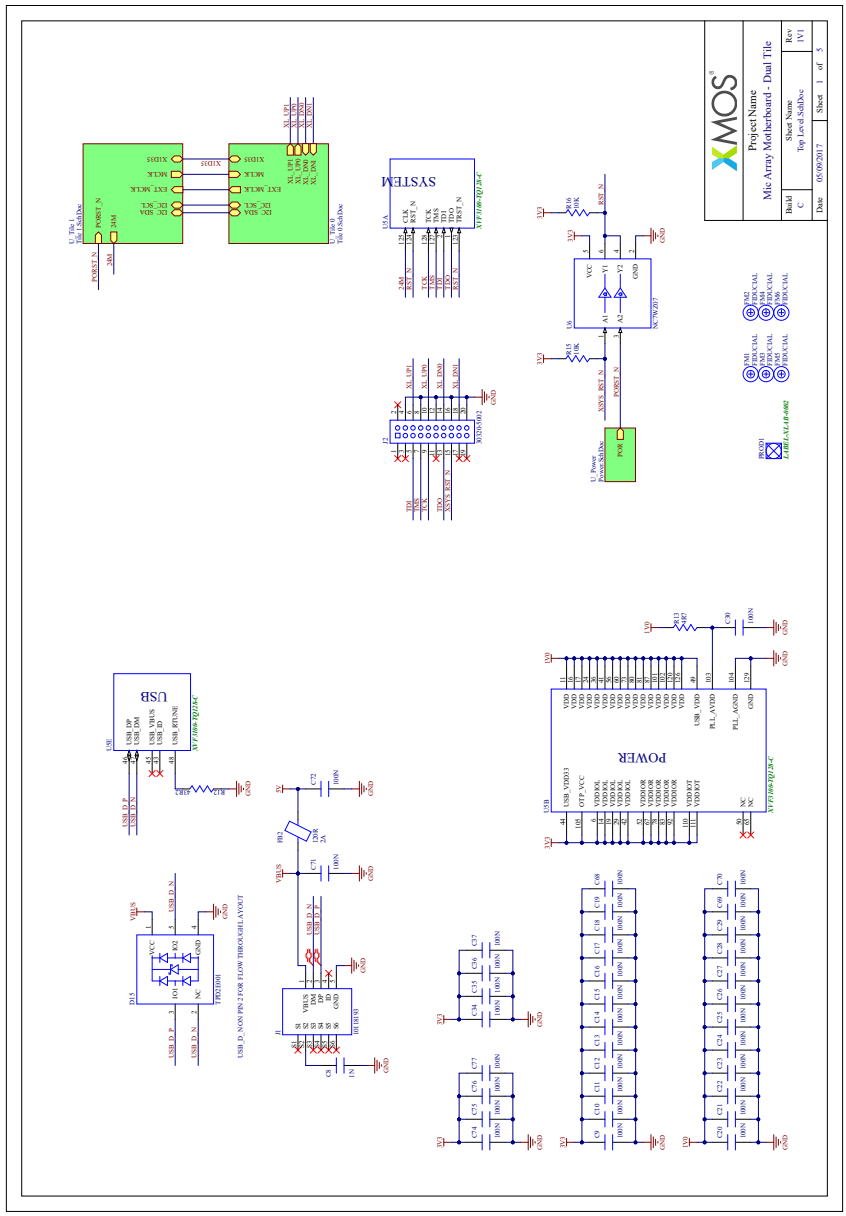

Figure 32: xCORE VocalFusion BaseBoard - XVF3100 configuration

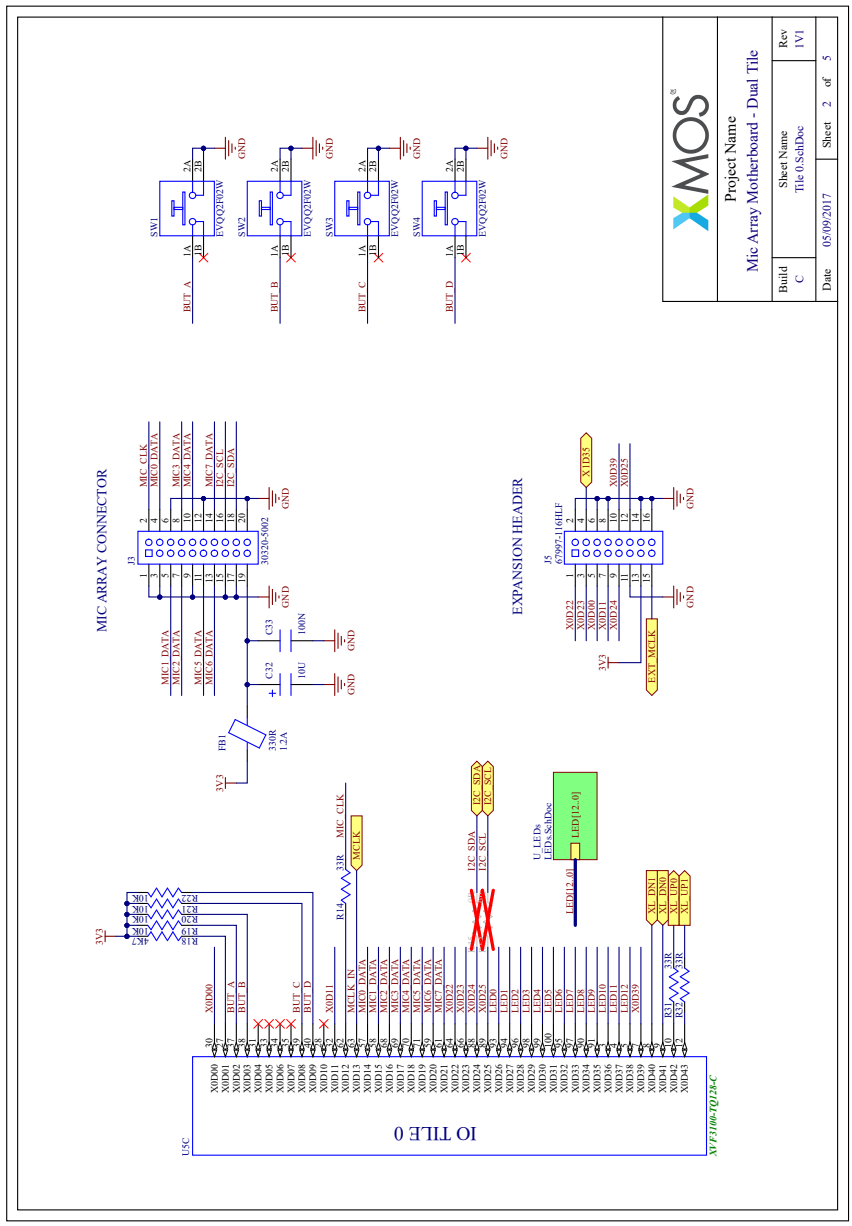

Figure 33: xCORE VocalFusion BaseBoard - extension header, buttons, Microphone header, Tile 0 IO

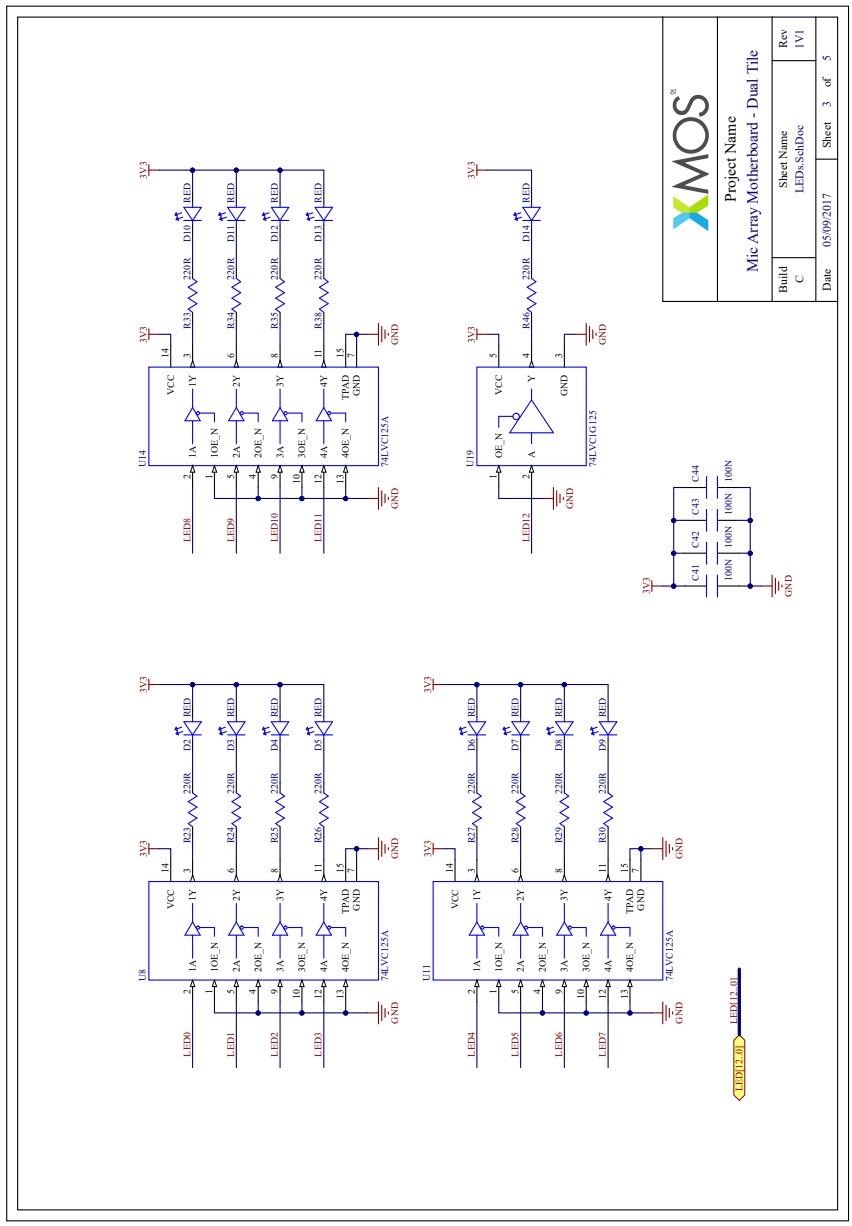

Figure 34: xCORE VocalFusion BaseBoard - LEDs

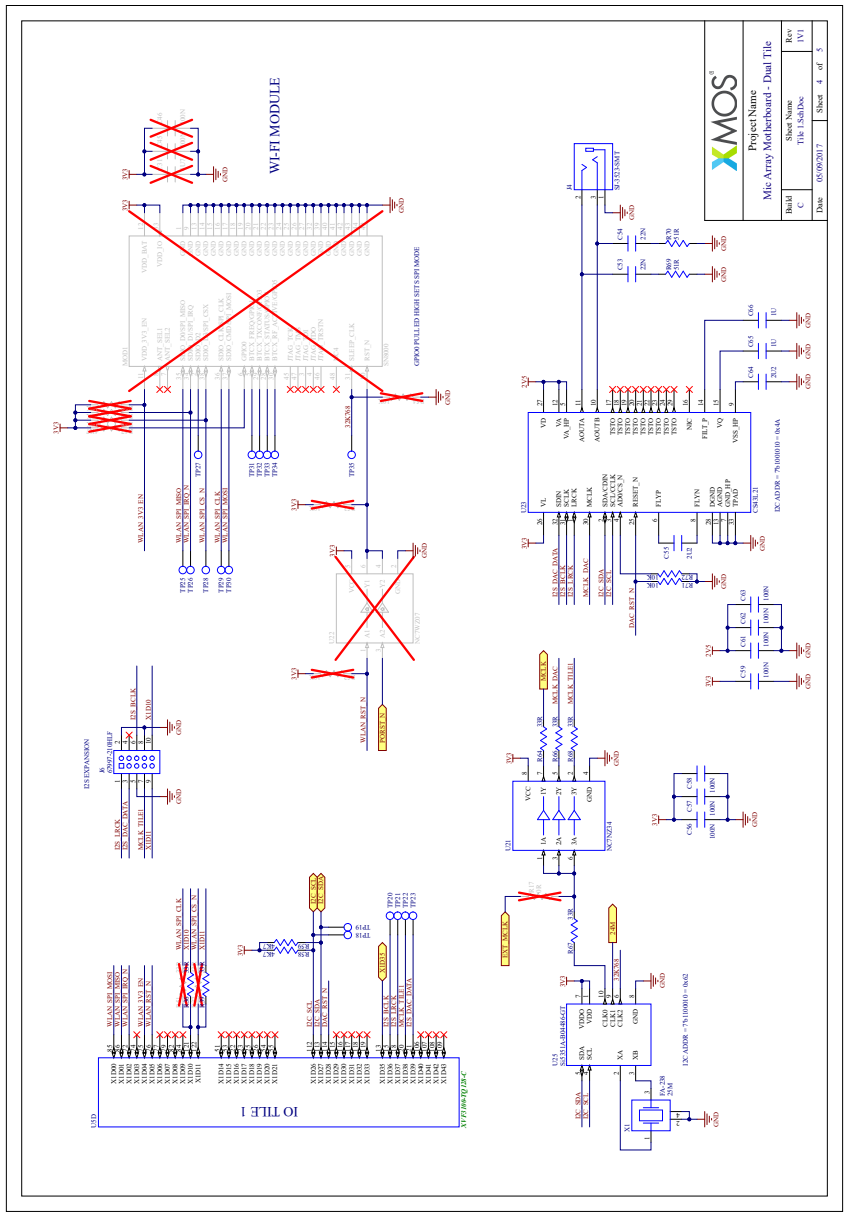

Figure 35: xCORE VocalFusion BaseBoard - Clock and stereo DAC with headphone jack circuitry, tile 1 IO

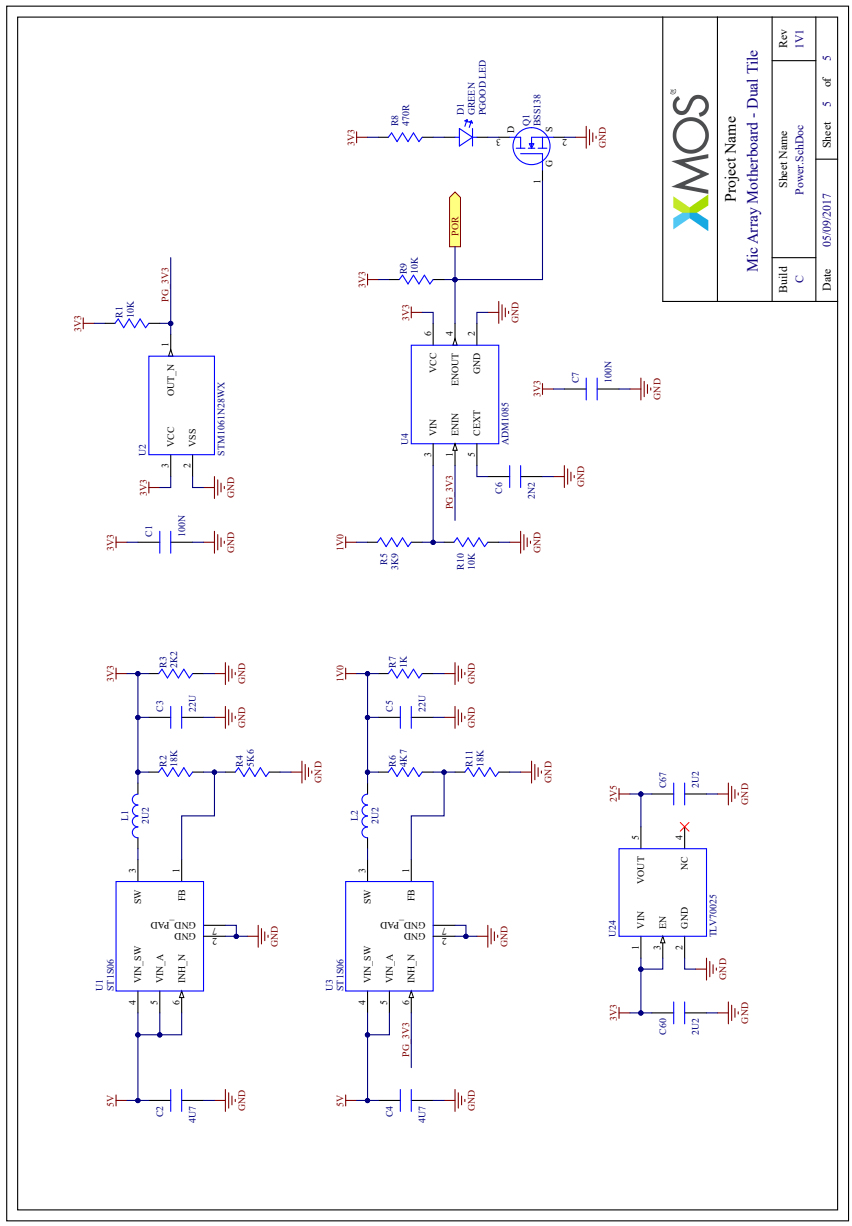

Figure 36: xCORE VocalFusion BaseBoard - voltage rail LDOs and reset circuit

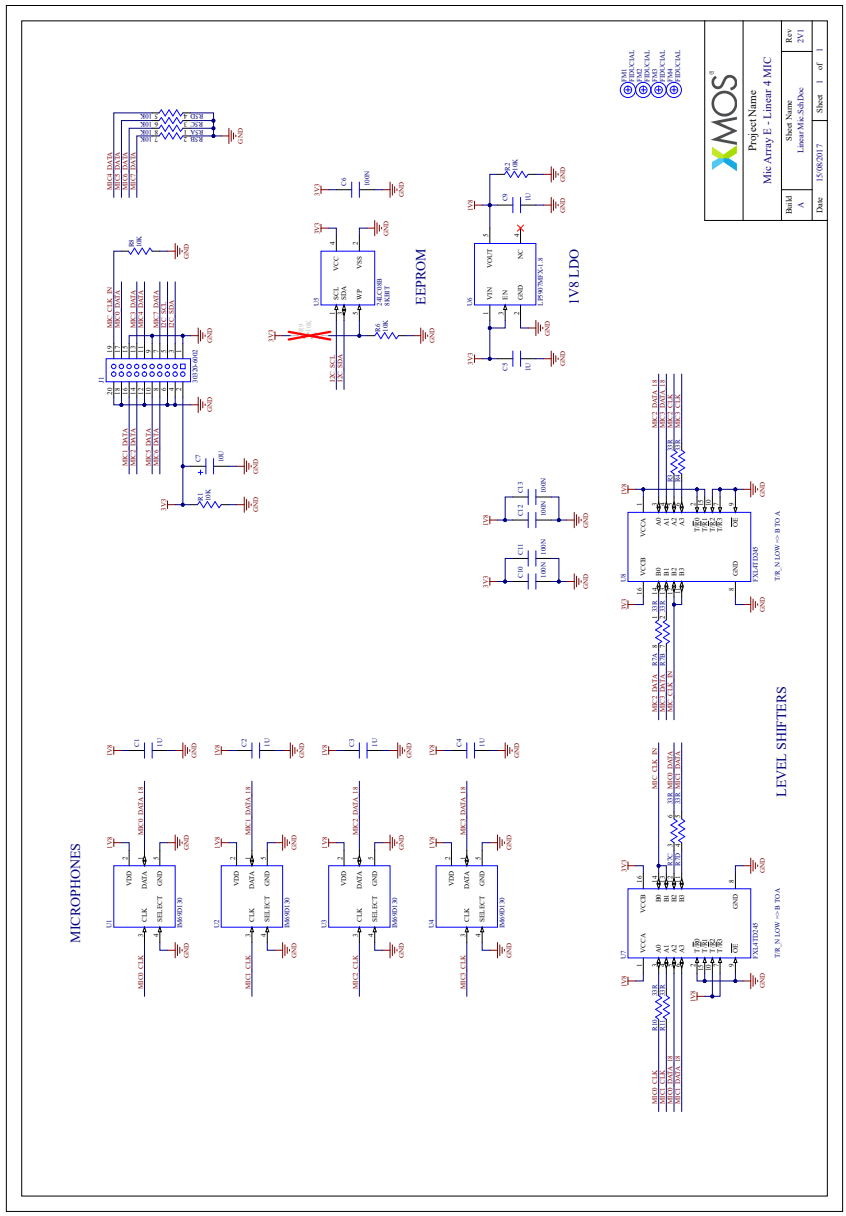

Figure 37: xCORE VocalFusion Speaker Linear Microphone Board

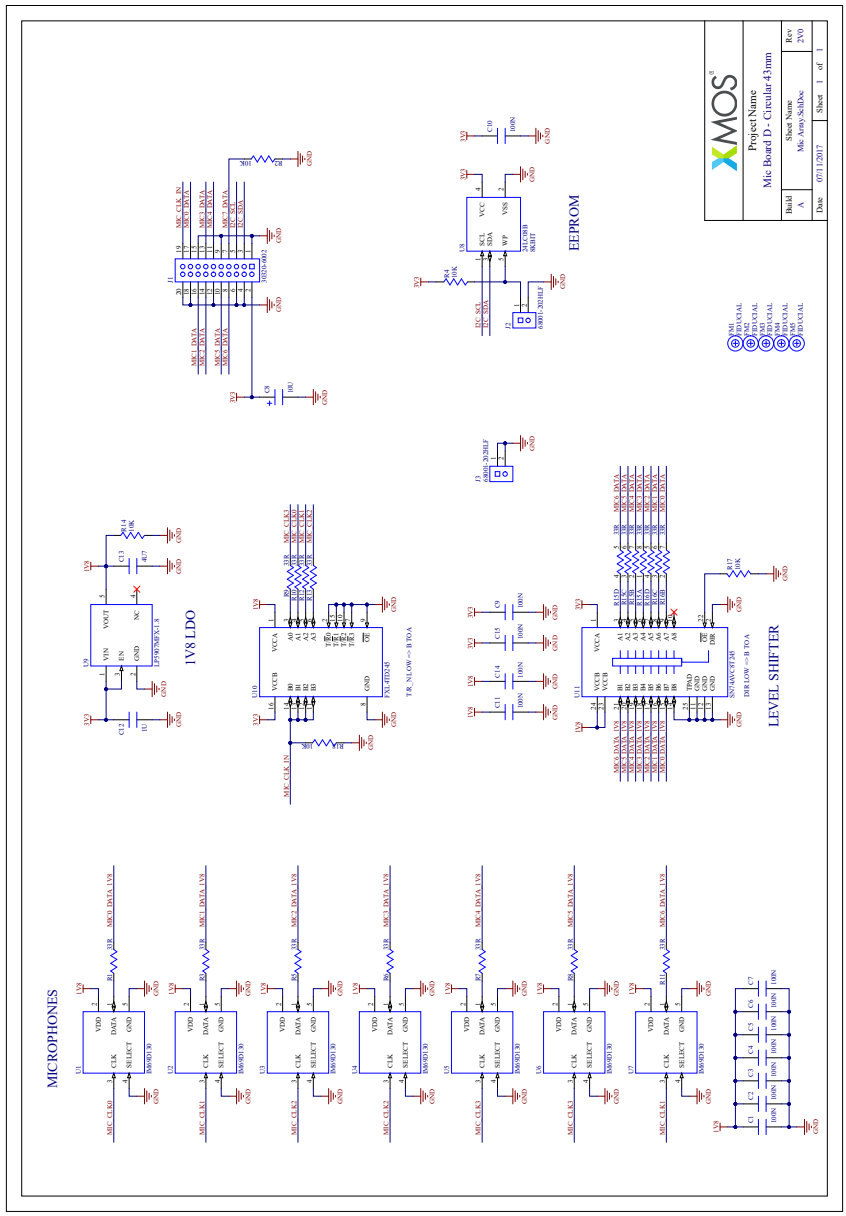

Figure 38: xCORE VocalFusion Speaker Circular Microphone board