xcore.ai Explorer v2 Board Manual

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XMOS

IN THIS DOCUMENT

The xcore.ai explorer board, XK-EVK-XU316, is an evaluation board for the xcore.ai cross-over processor from XMOS. The processor is easy to use and provides advanced features on a small, extremely low cost platform. This manual documents version 2 of the board.

xCORE lets you software-configure the interfaces that you need for your system; so with xcore.ai explorer board you can configure the board to match your exact requirements. The xcore.ai multicore microcontroller has sixteen 32bit logical cores, with single cycle floating point and vector operations. This makes xcore.ai explorer board an ideal platform for functions ranging from AI on the edge and robotics to networking and digital audio.

1 Introduction

The xcore.ai explorer board comprises an xcore.ai processor with a set of IO devices and connectors arranged around it, as shown in in Figure 1. Except for the flash, all components are optional, and are there to aid you in exploring the capabilities of the xcore.ai processor.

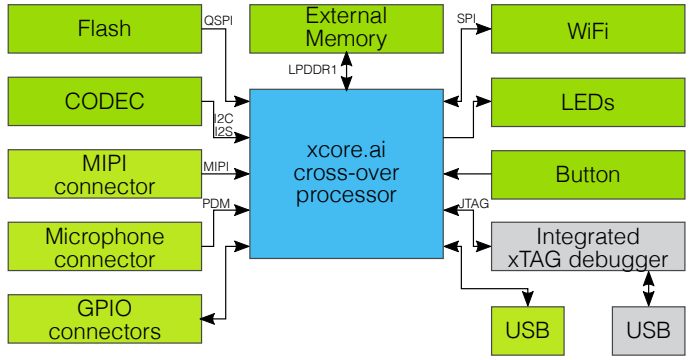

Figure 1: Block diagram of the explorer board

A Quick-Start guide, `http://xmos.ai/getting-started`, is available that has a few programs that you can run that show how to use the tool-chain and the libraries.

1.1 The xcore.ai Cross-Over Processor Device

The xcore.ai explorer board is based on a two-tile xcore.ai device (XU316-1024-FB265-C32), shown in Figure 2. Each tile is user-programmable, providing eight logical cores with a total of up to 1200 MIPS/MFLOPS compute, or 37 GMACC/s vector performance (other speed and temperature grades are available). A total of 58 general–purpose digital I/Os, distributed from both tiles, have been brought out to header pins, providing flexibility for connecting peripherals to the xcore.ai explorer board board.

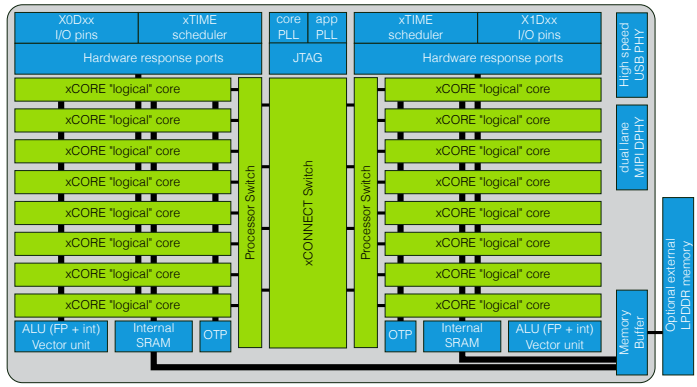

Figure 2: The xcore.ai XU316-1024-FB265-C32 device

For an introduction to xcore.ai tiles and cores see the xcore.ai Technical Overview, XM-014149-PC. For in depth information on the device see the XU316-1024-FB265 datasheet (XM-014035-PC or XM-014034-PC), and the XS3 Architecture Manual XM-014007-PS.

1.2 Board Features

A photo labelling the main elements of the xcore.ai explorer board is shown in Figure 3:

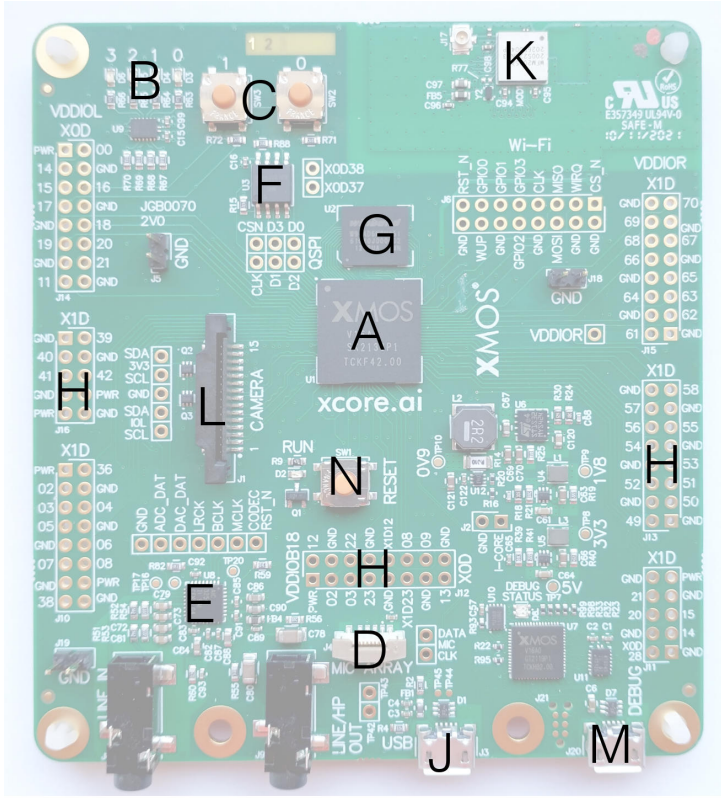

Figure 3: xcore.ai main components

The board includes the following features:

- A: The xcore.ai (XU316-1024-FB265-C32) Multicore Microcontroller device. XU316 identifies the Third generation XCORE with 16 threads and embedded USB; 1024 indicates 1 MByte of memory, FB265 indicates a 265-ball Fine Grid Ball Array, and C32 identifies this as an Commercial temperature device speed grade 600 MHz. Other packages, temperature, and speed grades are available.
- Board devices and GPIO:
  - B: Four general purpose LEDs
  - C: Two general purpose push-button switches

- D: A PDM microphone connector
- E: An audio codec with 3.5mm line-in and line-out connectors
- F: A QSPI flash, 32 Mbit
- G: An LPDDR1 external memory, 1 Gbit
- H: 58 GPIO connections from tile 0 and 1, arranged on 0.1” grids

- Connectivity:
  - J: A micro USB connector for power and connection to a USB host
  - K: A WiFi module with aerial.
  - L: A MIPI connector for connection to a MIPI camera

- Board support
  - M: An integrated xTAG4 debug adapter
  - N: A reset switch and a LED to indicate that the chip is running (not in reset)

2 Board devices and GPIO

2.1 User LEDs

The xcore.ai explorer board provides four LEDs on the top left corner of the board, as shown in Figure 4. The LEDs are active high, and are connected to the GPIO pins connected to port 4C on tile 0:

GPIO	Port	LED
X0D14	P4C0	0
X0D15	P4C1	1
X0D20	P4C2	2
X0D21	P4C3	3

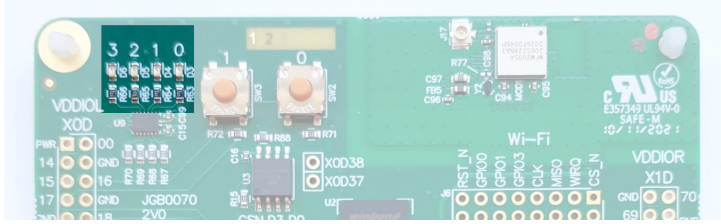

Figure 4: User LEDs

2.2 General purpose push-button switches

Two general purpose push-button switches are provided next to the LEDs as shown in Figure 5. When depressed, the push-buttons create a connection from the IO to GND. Care must be taken to ensure that this does not cause undesirable behaviour on the xcore.ai or other components connected through the GPIO headers.

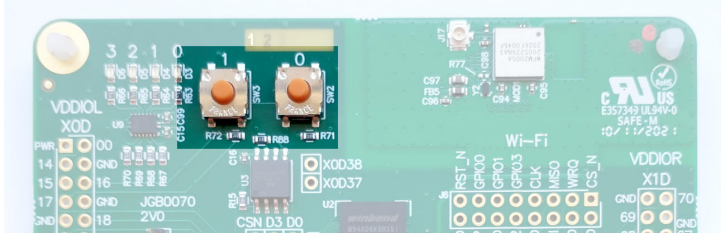

Figure 5: General purpose push-button switches

Each push-button switch is connected to a different IO on the xcore.ai device:

GPIO	Port	BUTTON
X0D16	P4D0	0
X0D17	P4D1	1

2.3 Microphone connector

Up to two PDM microphones can be connected to the xcore.ai explorer board. It uses a header that connects to XMOS microphone boards. It is located near the bottom of the board (J4), as shown in Figure 6, pinned out as follows:

Signal name	GPIO	Port	J4 Pin
VDDIOR			1
GND			2
MIC_CLK	X1D22	P1G	3
GND			4
MIC_DATA	X1D13	P1F	5
GND			6

There is a single microphone data line, for double data rate input. For example, a left microphone shall provide data on the rising edge of the clock, the right microphone shall provide data on the falling edge of the clock. If only one microphone is connected, one of the edges can be ignored. Note that the microphone is supplied from VDDIOR, which is 3V3 on an unmodified board (see §4.3 for details on how to modify the IO voltages)

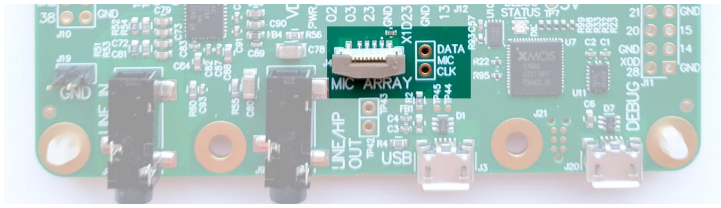

Figure 6: Microphone connector

2.4 Audio codec

The xcore.ai explorer board provides a stereo codec (TLV320AIC3254) on the bottom left of the board, Figure 7. It is connected to the xcore.ai chip via I2C and I2S interfaces:

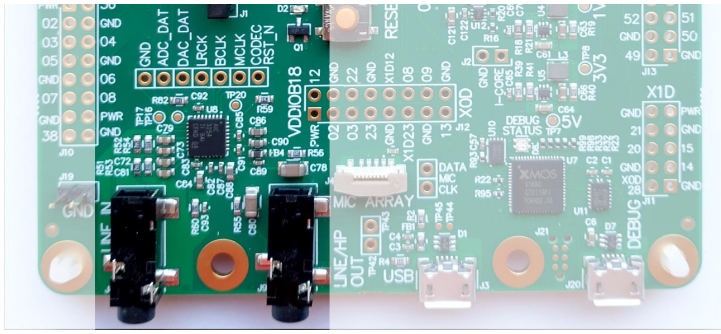

Figure 7: CODEC

GPIO	Port	signal
X0D37	P1N	I2C_SCL
X0D38	P1O	I2C_SDA
X1D11	P1D	I2S_MCLK
X1D01	P1B	I2S_LRCLK
X1D10	P1C	I2S_BCLK
X1D00	P1A	I2S_DAC_DATA
X1D37	P1N	I2S_ADC_DATA
X1D09	P4A3	CODEC_RESET

The I2S signals are on the VDDIOR domain, the I2C signals are on the VDDIOL domain but are routed through level shifters, enabling the CODEC to use VDDIOR for its I/O voltage.

The master clock, which is provided to both the xcore.ai and the CODEC for synchronisation, is generated by a PLL that is integrated in the xcore.ai device, see XM-014200-AN for more details.

2.5 QSPI Flash

The xcore.ai explorer board includes 4 Mbytes of external Quad Serial Peripheral Interface (QSPI) FLASH memory, which is interfaced by the GPIO connections as per the standard prescribed in the datasheet:

GPIO	Port	QSPI connection
X0D01	P1B	CS_N
X0D04	P4B0	IO0
X0D05	P4B1	IO1
X0D06	P4B2	IO2
X0D07	P4B3	IO3
X0D10	P1C	SPI_CLK

The XTC tools include the xFLASH utility for programming compiled programs into the flash memory. xcore.ai applications may also access the FLASH memory at run-time by interfacing through those ports.

2.6 LPDDR memory

The xcore.ai explorer board includes 128 Mbytes of external LPDDR memory. They are connected as documented in the application note on xcore.ai External LPDDR Memory, XM-014230-AN.

2.7 GPIO headers (J10-J16)

Most of the GPIO are brought out on headers J10-J16 so that external devices can be connected to the explorer board. The connectors are along the left hand side of the

board (these are all at VDDIOL voltage levels), the right hand side of the board (these are all at VDDIOR voltage levels), and the middle bottom of the board (a few GPIO at 1V8), see Figure 8.

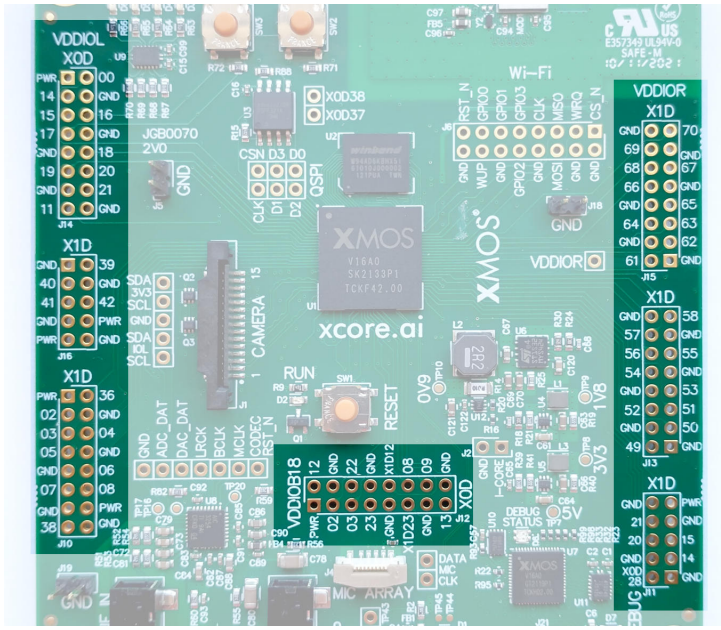

Figure 8: GPIO connectors

The xCORE pins are mapped to the GPIO connector pins as shown below. The three connectors on the left are powered through VDDIOL. GPIO connector J10 (Tile 1):

Signal	Port	Pin	Signal	Port	Pin
VDDIOL		1	X1D36	P1M	2
X1D02	P4A0	3	GND		4
X1D03	P4A1	5	X1D04	P4B0	6
X1D05	P4B1	7	GND		8
GND		9	X1D06	P4B2	10
X1D07	P4B3	11	X1D08	P4A2	12
GND		13	VDDIOL		14
X1D38	P1O	15	GND		16

GPIO connector J14 (Tile 0). Note: the two pins marked “+” are also connected to a button:

Signal	Port	Pin	Signal	Port	Pin
VDDIOL		1	X0D00	P1A	2
X0D14	P4C0	3	GND		4
X0D15	P4C1	5	X0D16	P4D0 +	6
X0D17	P4D1 +	7	GND		8
GND		9	X0D18	P4D2	10
X0D19	P4D3	11	X0D20	P4C2	12
GND		13	X0D21	P4C3	14
X0D11	P1D	15	GND		16

GPIO connector J16 (Tile 1):

Signal	Port	Pin	Signal	Port	Pin
GND		1	X1D39	P1P	2
X1D40	P8D4	3	GND		4
X1D41	P8D5	5	X1D42	P8D6	6
GND		7	VDDIOL		8
VDDIOL		9	GND		10

The three connectors on the right are powered through VDDIOR. GPIO connector J11 (Tile 1 and Tile 0):

Signal	Port	Pin	Signal	Port	Pin
GND		1	X0D28	P4F0	2
X1D14	P4C0	3	GND		4
X1D15	P4C1	5	X1D20	P4C2	6
GND		7	X1D21	P4C3	8
VDDIOR		9	GND		10

GPIO connector J13 (Tile 1):

Signal	Port	Pin	Signal	Port	Pin
GND		1	X1D49	P32A0	2
X1D50	P32A1	3	GND		4
X1D51	P32A2	5	X1D52	P32A3	6
X1D53	P32A4	7	GND		8
GND		9	X1D54	P32A5	10
X1D55	P32A6	11	X1D56	P32A7	12
GND		13	X1D57	P32A8	14
X1D58	P32A9	15	GND		16

GPIO connector J15 (Tile 1):

Signal	Port	Pin	Signal	Port	Pin
GND		1	X1D61	P32A10	2
X1D62	P32A11	3	GND		4
X1D63	P32A12	5	X1D64	P32A13	6
X1D65	P32A14	7	GND		8
GND		9	X1D66	P32A15	10
X1D67	P32A16	11	X1D68	P32A17	12
GND		13	X1D69	P32A18	14
X1D70	P32A19	15	GND		16

GPIO connector J12, just below the device is powered from 1V8, and has IO from tile 0 and tile 1:

Signal	Port	Pin	Signal	Port	Pin
1V8		1	X0D12	P1E	2
X0D02	P4A0	3	GND		4
X0D03	P4A1	5	X0D22	P1G	6
X0D23	P1H	7	GND		8
GND		9	X1D12	P1E	10
X1D23	P1H	11	X0D08	P4A2	12
GND		13	X0D09	P4A3	14
X0D13	P1F	15	GND		16

Electrical characteristics of all I/O pins are detailed in the datasheet, XM-014035-PC.

3 Standard connectivity options

The board has provision to be connected to a host computer through USB, to the internet over WiFi, or to a camera over MIPI.

3.1 USB

There is a micro-USB (B-type) connector (J3) along the bottom of the board, Figure 9.

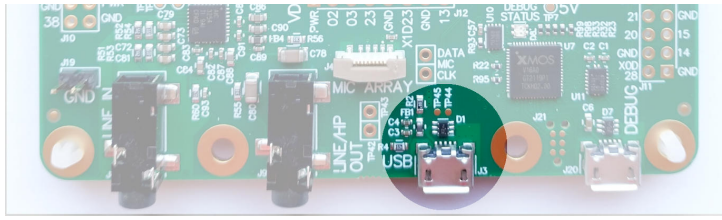

Figure 9: USB connector

J3 must be connected at all times, to provide power to the xcore.ai explorer board.

3.2 WiFi

A Silicon Labs WFM200SA WiFi module is integrated on the top right-hand corner of the board, Figure 10. An aerial is included on the PCB, an external aerial can be connected to J17 if required. The WiFi module is connected to the xcore.ai chip via a SPI interface as follows:

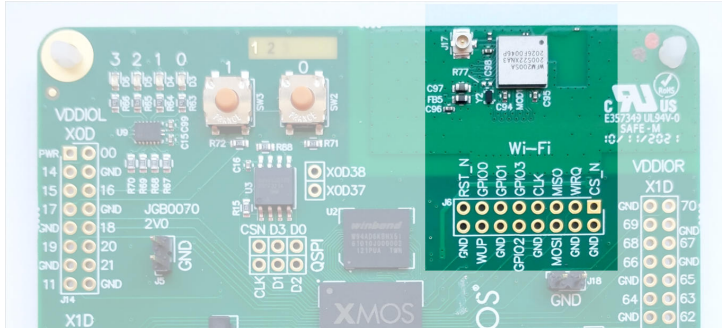

Figure 10: WiFi module

GPIO	Port	signal
X0D35	P1L	WIFI_SPI_CLK
X0D25	P1J	WIFI_SPI_MOSI
X0D36	P1M	WIFI_SPI_MISO
X0D29	P4F1	WIFI_SPI_CS_N
X0D27	P4E1	WIFI_RST_N
X0D24	P1I	WIFI_WIRQ
X0D26	P4E0	WIFI_WUP

3.3 MIPI

The MIPI interface is brought out on a connector that is compatible with RaspberryPi V2 cameras, Figure 11. When you plug an flat-flexi cable in, the contacts should be facing the xcore.ai device. In order to use it with a standard MIPI camera, you must configure the MIPI interface on the xcore.ai device as follows:

- Swap the Positive and Negative wires on all lanes
- Select lane two to be the clock lane.

See the xcore.ai MIPI application note, XM-014203-AN, for details. Either a single or dual data lanes can be used, as supported by the camera. The pin-out of the connector to the xcore.ai device is as follows:

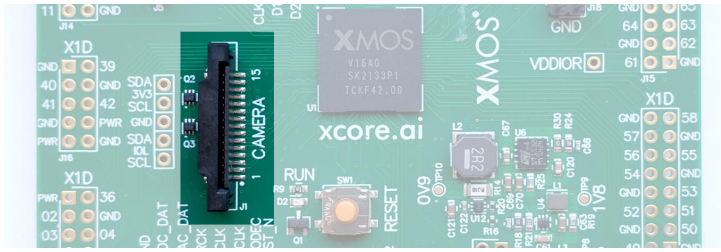

Figure 11: MIPI connector

GPIO	Connector signal	xcore.ai
1A	GND	
2A	MIPI_D0_N	MIPI_D0_P
3A	MIPI_D0_P	MIPI_D0_N
4A	GND	
5A	MIPI_D1_N	MIPI_D1_P
6A	MIPI_D1_P	MIPI_D1_N
7A	GND	
8A	MIPI_CLK_N	MIPI_D2_P
9A	MIPI_CLK_P	MIPI_D2_N
10A	GND	
11A	GPIO	3V3 pull-up
12A	GND	
13A	SCL (at 3V3)	X0D37
14A	SDA (at 3V3)	X0D38
15A	3V3	

4 Board support

The board comes with a debug adapter, oscillator, and power supplies.

4.1 xTAG4 debugger

The board has an on-board debugger that is available through the a micro-USB (B-type) connector along the bottom of the board, Figure 12.

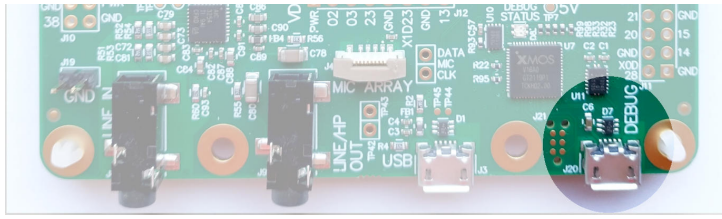

Figure 12: Debug USB connector

The xTAG debugger allows the XTC tools to interrogate the application running on the xcore.ai device using the XMOS debugger and the xSCOPE library which provides non-intrusive program instrumentation.

4.2 24MHz Crystal Oscillator

The xcore.ai explorer board board is clocked at 24 MHz by a crystal oscillator, the xcore.ai device contains the oscillator, the board has a 24 MHz crystal.

4.3 Power and Operating Requirements

The xcore.ai explorer board requires a 5V power source that is normally provided through the micro-USB cable J3. The voltage is converted by on-board regulators to the 0V9, 1V8 and 3V3 supplies used by the components.

To ease measurements of core current the board includes a sense-amp. You can measure the current by putting a voltmeter across J2. A 1V reading on J2 is equivalent to 500 mA core current (450 mW at 0.9V).

By default, VDDIOL and VDDIOR are powered at 3V3. If you need different voltage levels you can change the following:

- You can make VDDIOL 1V8 by removing R35, and soldering 0R resistors on R5 and R36.
- You can make both VDDIOL and VDDIOR 1V8 by removing R35 and R37. and soldering 0R resistors on R5, R6, R36, and R38

The table below summarises the default state of the VDDIO power supplies (row 1), and resistors that can be added or removed in order to change the VDDIO supply voltages.

VDDIOL	VDDIOR	R5	R6	R35	R36	R37	R38
3V3	3V3	DNF	DNF	Fitted	DNF	Fitted	DNF
1V8	3V3	Added	DNF	Removed	Added	Fitted	DNF
1V8	1V8	Added	Added	Removed	Added	Removed	Added

Changing the resistors to operate at 1V8 must be done with care as incorrect settings may damage the device. The resistors are located on the back of the board as shown in Figure 13.

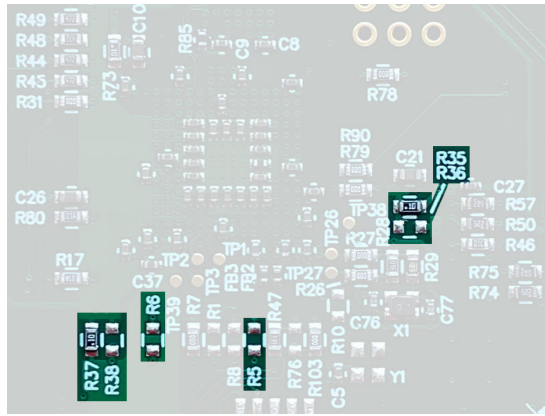

Figure 13: Resistors that govern VDDIO on the back of the board.

Making VDDIOR 1V8 whilst VDDIOL stays 3V3 is not an option that is supported by the board schematics. The level shifters in the I2C lines that make I2C work at both 3V3 and 1V8 only work on the two configurations shown.

5 Mechanical and Environmental Specifications

The xcore.ai explorer board dimensions are 100 x 90mm. The mounting holes are 3.2mm in diameter. The board should be operated at between 0 and 70C.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the xcore.ai explorer board with appropriate ESD precautions in place.

6 Compliance

6.1 RoHS and REACH

The xcore.ai explorer board complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The xcore.ai explorer board is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU. See also

- `https://www.xmos.ai/environmental`

7 Further information

Document title	Link and document number
XU316-1024-FB265 datasheet	XM-014035-PC
XU316-1024-QF60A datasheet	XM-014034-PC
The XS3 Architecture Manual	XM-014007-PS

Note that this board contains the FB265 BGA package that brings out all GPIO. Smaller packages such as the referenced QF60A package are available.

8 Part Numbers and Board Markings

Part number	Board marking
XK-EVK-XU316	JGB0070 2V0

9 Revision History

Date	Release	Comment
2024-02-12	2.0	Version 2 of board schematics
2022-06-24	1.0	First release

Appendix A Full port map

Pin	Port	Signal
X0D00	P1A	GPIO
X0D01	P1B	CS_N
X0D02	P4A0	GPIO
X0D03	P4A1	GPIO
X0D04	P4B0	IO0
X0D05	P4B1	IO1
X0D06	P4B2	IO2
X0D07	P4B3	IO3
X0D08	P4A2	GPIO
X0D09	P4A3	GPIO
X0D10	P1C	SPI_CLK
X0D11	P1D	GPIO
X0D12	P1E	GPIO
X0D13	P1F	GPIO
X0D14	P4C0	GPIO
X0D14	P4C0	GPIO
X0D15	P4C1	GPIO
X0D15	P4C1	GPIO
X0D16	P4D0	GPIO
X0D16	P4D0 +	GPIO
X0D17	P4D1	GPIO
X0D17	P4D1 +	GPIO
X0D18	P4D2	GPIO
X0D19	P4D3	GPIO
X0D20	P4C2	GPIO
X0D20	P4C2	GPIO
X0D21	P4C3	GPIO
X0D21	P4C3	GPIO
X0D22	P1G	GPIO
X0D23	P1H	GPIO
X0D24	P1I	WIFI_WIRQ
X0D25	P1J	WIFI_SPI_MOSI
X0D26	P4E0	WIFI_WUP
X0D27	P4E1	WIFI_RST_N
X0D28	P4F0	GPIO
X0D29	P4F1	WIFI_SPI_CS_N
X0D35	P1L	WIFI_SPI_CLK
X0D36	P1M	WIFI_SPI_MISO
X0D37	P1N	I2C_SCL

(continued)

Pin	Port	Signal
X0D37	P1N	SCL (at 3V3)
X0D38	P1O	I2C_SDA
X0D38	P1O	SDA (at 3V3)
X1D00	P1A	I2S_DAC_DATA
X1D01	P1B	I2S_LRCLK
X1D02	P4A0	GPIO
X1D03	P4A1	GPIO
X1D04	P4B0	GPIO
X1D05	P4B1	GPIO
X1D06	P4B2	GPIO
X1D07	P4B3	GPIO
X1D08	P4A2	GPIO
X1D09	P4A3	CODEC_RESET
X1D10	P1C	I2S_BCLK
X1D11	P1D	I2S_MCLK
X1D12	P1E	GPIO
X1D13	P1F	MIC_DATA
X1D14	P4C0	GPIO
X1D15	P4C1	GPIO
X1D20	P4C2	GPIO
X1D21	P4C3	GPIO
X1D22	P1G	MIC_CLK
X1D23	P1H	GPIO
X1D36	P1M	GPIO
X1D37	P1N	I2S_ADC_DATA
X1D38	P1O	GPIO
X1D39	P1P	GPIO
X1D40	P8D4	GPIO
X1D41	P8D5	GPIO
X1D42	P8D6	GPIO
X1D49	P32A0	GPIO
X1D50	P32A1	GPIO
X1D51	P32A2	GPIO
X1D52	P32A3	GPIO
X1D53	P32A4	GPIO
X1D54	P32A5	GPIO
X1D55	P32A6	GPIO
X1D56	P32A7	GPIO
X1D57	P32A8	GPIO
X1D58	P32A9	GPIO
X1D61	P32A10	GPIO

(continued)

Pin	Port	Signal
X1D62	P32A11	GPIO
X1D63	P32A12	GPIO
X1D64	P32A13	GPIO
X1D65	P32A14	GPIO
X1D66	P32A15	GPIO
X1D67	P32A16	GPIO
X1D68	P32A17	GPIO
X1D69	P32A18	GPIO
X1D70	P32A19	GPIO

Appendix B Board Schematics

The schematics are shown in Figure 14 .. Figure 22.

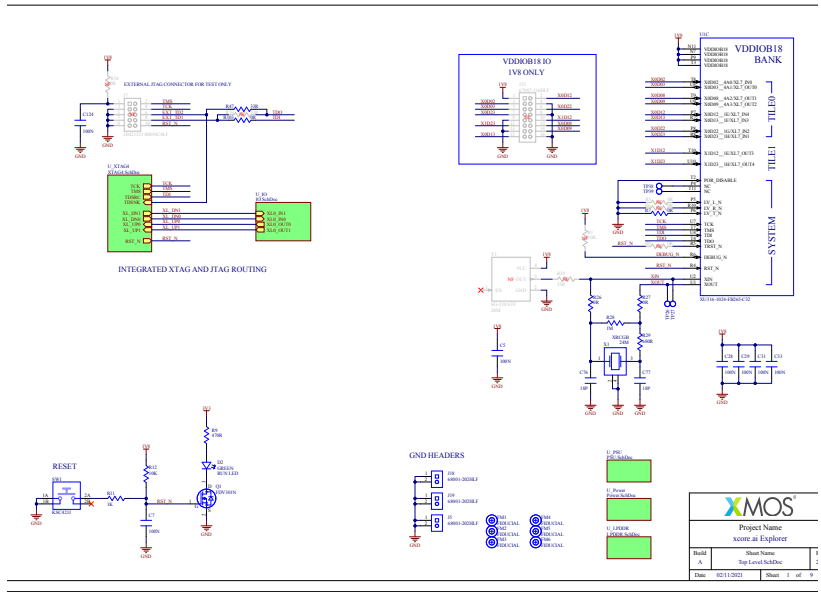

Figure 14: xcore.ai explorer board system schematic

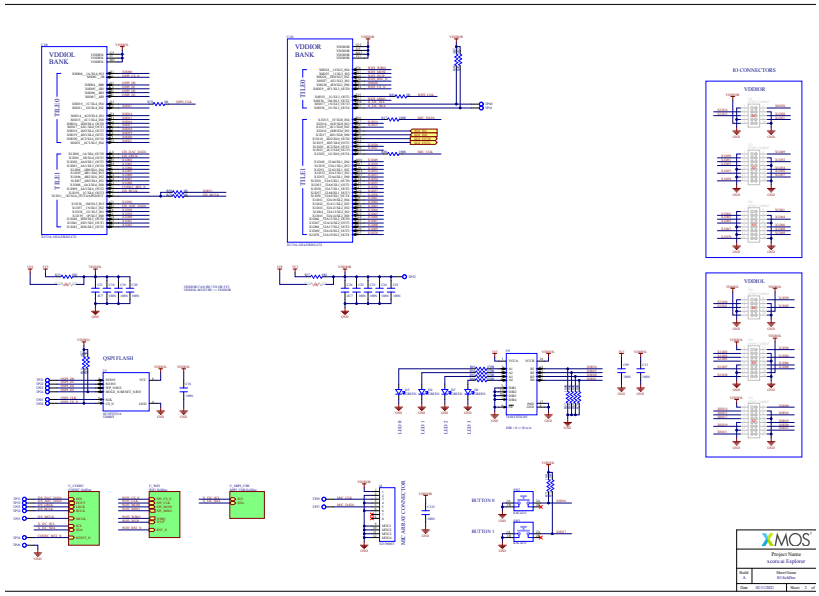

Figure 15: xcore.ai explorer board GPIO schematic

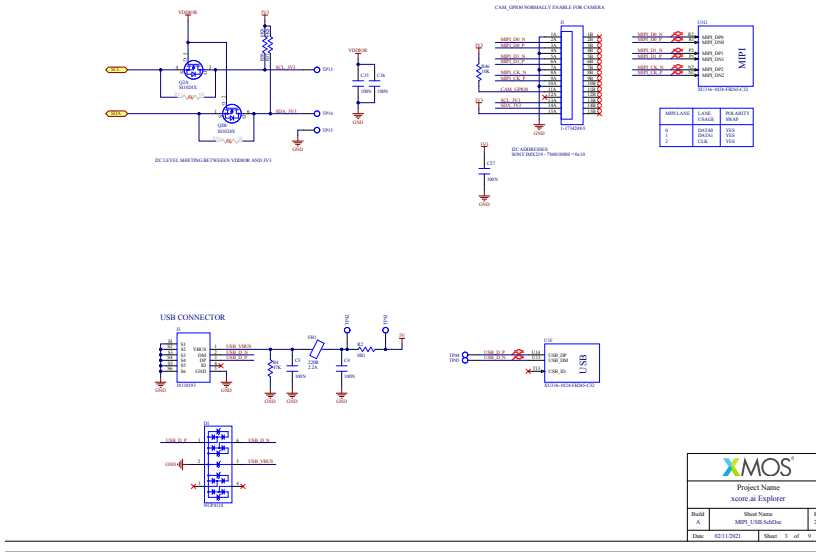

Figure 16: xcore.ai explorer board MIPI/USB schematic

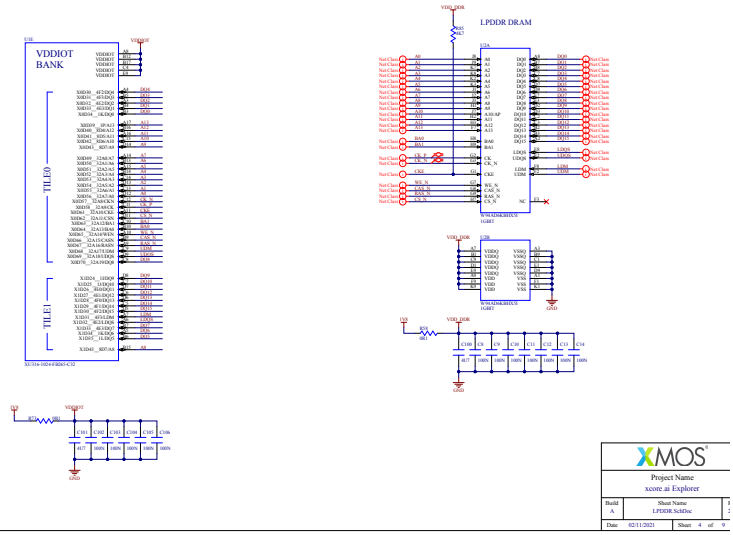

Figure 17: xcore.ai explorer board LPDDR schematic

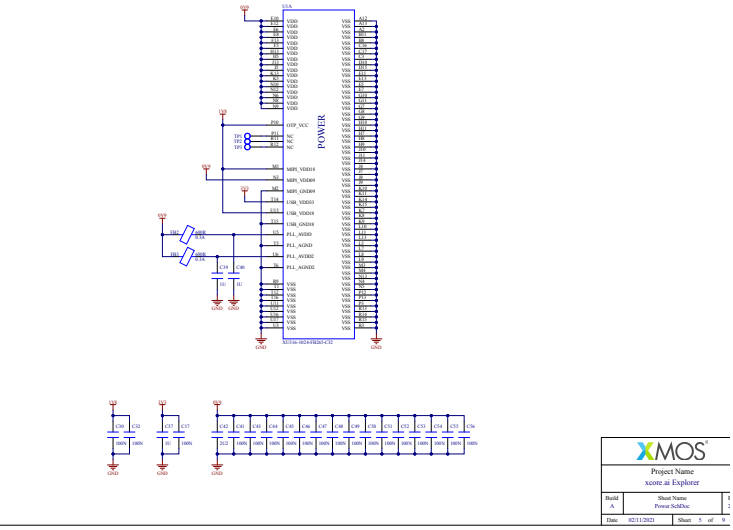

Figure 18: xcore.ai explorer board supply decoupling schematic

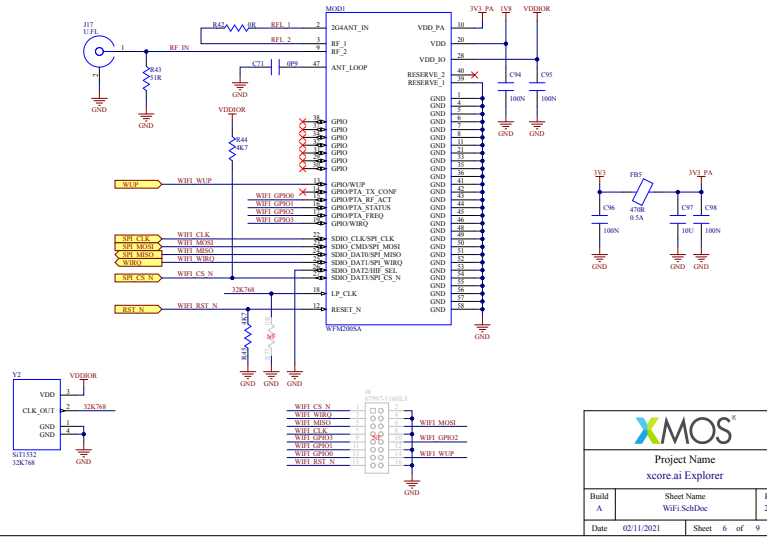

Figure 19: xcore.ai explorer board WiFi schematic

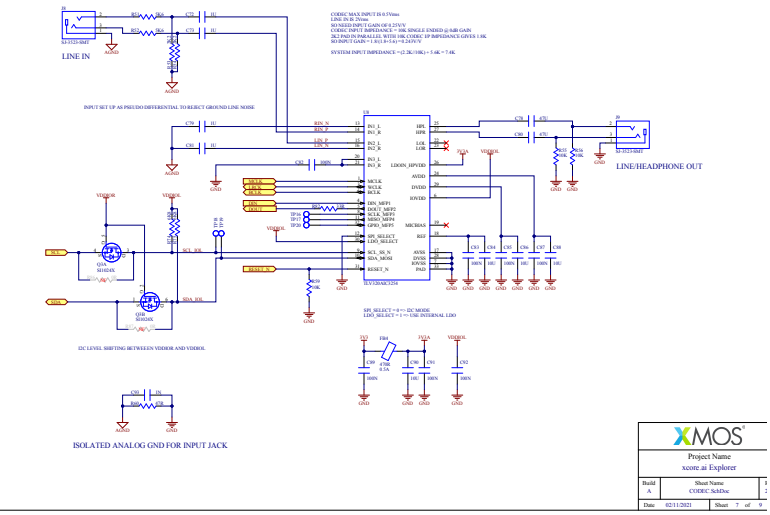

Figure 20: xcore.ai explorer board codec schematic

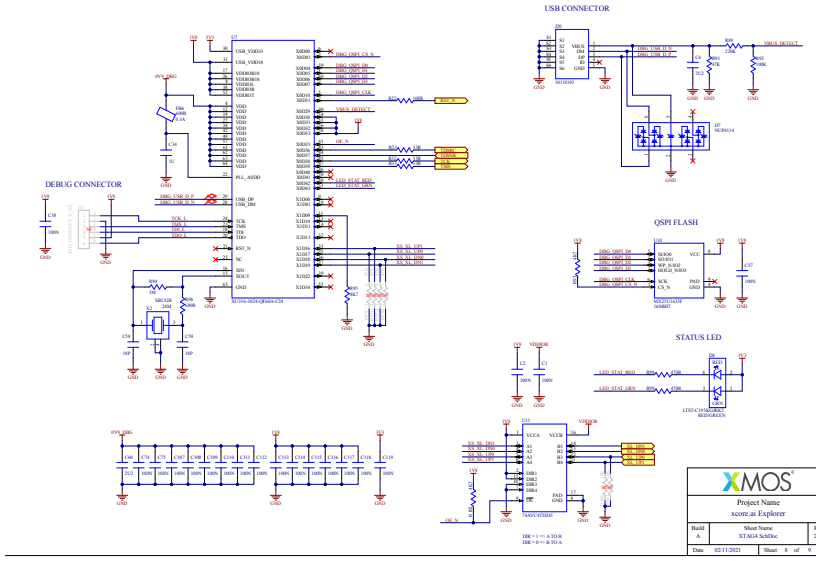

Figure 21: xcore.ai explorer board integrated XTAG4 schematic

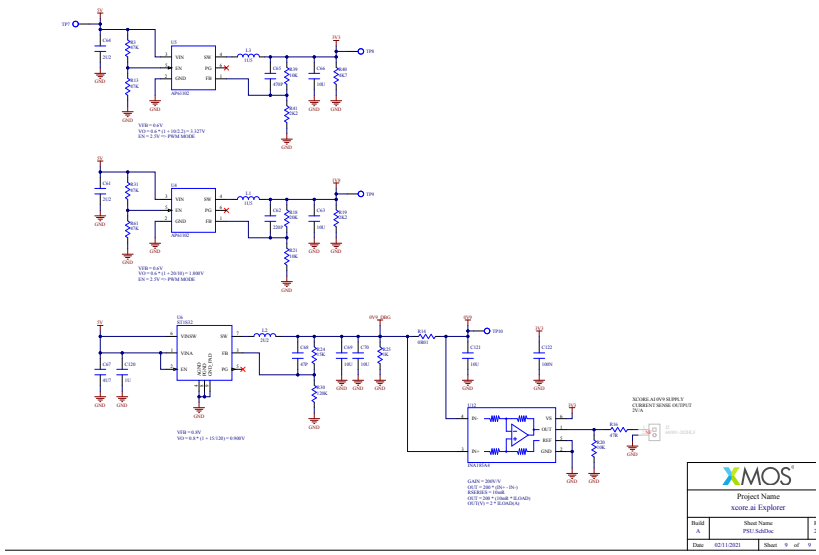

Figure 22: xcore.ai explorer board power schematic