SDRAM Library

The XMOS SDRAM library is designed for read and write access of arbitrary length 32b long word buffers at up to 62.5MHz clock rates. It uses an optimized pinout with address and data lines overlaid along with other pinout optimizations to implement 16 bit read/writes to Single Data Rate (SDR) SDRAM devices of size up to 256Mb, while consuming a total of just 20 xCORE I/O pins.

Features

The SDRAM component has the following features:

- Configurability of:
  - SDRAM capacity
  - clock rate (62.5 to 25MHz steps are provided)
  - refresh properties
- Supports:
  - read of 32b long words
  - write of 32b long words
  - one or more clients
  - asynchronous command decoupling with a command queue of length 8 for each client
  - refresh handled by the SDRAM component itself
- Requires a single core for the server
- Requires 500MHz core clock operation

Components

- SDRAM server
- Memory address allocator

Resource Usage

This following table shows typical resource usage in some different configurations. Exact resource usage will depend on the particular use of the library by the application.

Configuration	Pins	Ports	Clocks	Ram	Logical cores
SDRAM server	20	4 (1-bit), 1 (16-bit)	1	~4.0K	1
Memory address allocator	0	0	0	~0.3K	0

Software version and dependencies

This document pertains to version 3.2.0 of this library. It is known to work on version 14.3.0 of the xTIMEcomposer tools suite, it may work on other versions.

The library does not have any dependencies (i.e. it does not rely on any other libraries).

Related application notes

- I/O Timings for xCORE200[1].

[1] https://www.xmos.com/download/private/I-O-timings-for-xCORE200%281.0%29.pdf