Application Note: AN01005

Estimating Power Consumption For XS1-L Devices

This application note discusses the methodology for estimating total average power consumption of XS1-L devices. Power estimates are based on characterization data measured over power supply voltage, xCORE tile frequency (CLK), and junction temperature (TJ).

1 Overview

The total power consumption of the XS1-L processor is the sum of the power consumed for both of the power supply domains, VDD(CORE) and VDD(IO). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using XS1-L multicore microcontrollers. It provides a breakdown of the elements of the VDD(CORE) and VDD(IO) load and a simple worked example. Please consult the following sections of device specific datasheets for details discussed in this application note:

Operating Conditions for details regarding VDD(CORE) and VDD(IO) ranges

Ordering Guide for a comprehensive list of the available speed and temperature grade models

1.1 Internal power consumption

The total power consumption due to internal circuitry (on the VDD(CORE) supply) is the sum of the static power component and dynamic power component of each processor and each switch's core logic.

The dynamic portion of the xCORE internal power depends in varying degrees on the operating frequency, the instruction execution sequence, the data operands involved, and the instruction rate. The dynamic portion of the switch power depends on the operating frequency, amount of communication activity and the data itself. In both cases the static portion of the internal power is a function of temperature and voltage; it is not related to processor or switch activity.

XMOS provides current consumption figures for the incremental system utilization scenarios shown in Table 1. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for XS1-L processors in a given application.

Component	**Description**
IDD-DYN-PLL	Dynamic power consumption of the on-chip PLL.
IDD-DYN-STATIC	Leakage current during dynamic operation.
IDD-DYN-BASE	The base dynamic power consumption of one xCORE running a typical instruction sequence, with minimal resource use.
IDD-DYN-BUSY	The *incremental*, *additional* dynamic power consumption when the instruction pipeline is fully active with an aggressive instruction sequence (for example, four threads running with minimum stalls to wait for event completion), over and above IDD-DYN-BASE
IDD-DYN-RSRC	The *incremental*, *additional* dynamic power consumption when a full complement of port resources (sufficient to utilize all the general purpose I/O) and timers are enabled. Few applications will actually use this amount of resources so this component can be regarded as an upper bound for resource usage.
IDD-DYN-SWITCH	The *incremental*, *additional* dynamic power consumption when the system switch is enabled for inter-core (XS1-L16) or inter-chip (XS1) communication using XMOS Links.

Table 1: Internal power vectors

2 Calculating Application Specific Internal Power Consumption

The power vectors from Table 1 are all measured and expressed for a nominal VDD of 1V and measure on typical silicon. The total current consumption of the XS1 device can be calculated by simply summing the vectors which are appropriate for the application.

2.1 Static Power Consumption

The leakage profile of the XS1-L is shown below.

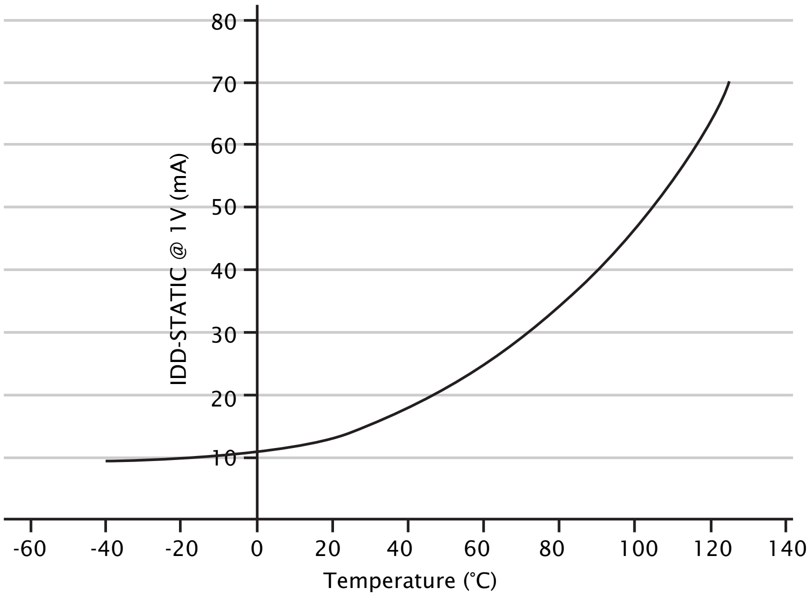

Figure 1: IDD-DYN-STATIC vs Temperature

2.2 PLL Power Consumption

The on-chip PLL consumes 6.5mA when VDD is 1V and the PLL is using the XS1-L default settings (after reset). Altering PLL settings such that its internal VCO frequency is changed, results in minor deviations from this default PLL power consumption.

2.3 Base Power Consumption

Total power consumption estimates for all applications should incorporate the IDD-DYN-STATIC and IDD-DYN-BASE vectors.

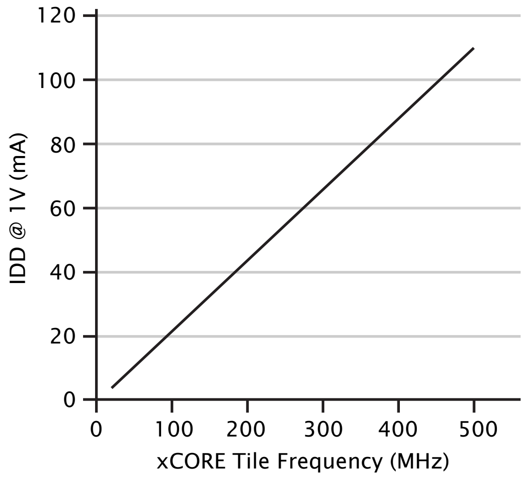

Figure 2: IDD-DYN-BASE vs Frequency

2.4 System Switch Power Consumption

If the system switch is used to communicate between multiple XS1 devices, the IDD-DYN-SWITCH component should also be incorporated according to the frequency at which the system switch is going to be run.

The system switch clock is derived as an integer division (which may be 1) from the internal PLL. The maximum divider is 256, which with the PLL output set to 500MHz would give a 2MHz system switch speed. Applications which will never use the system switch may therefore set the divider to this maximum value[1].

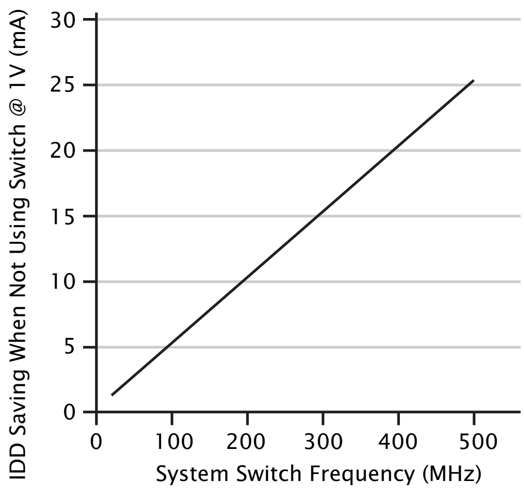

Figure 3: IDD-DYN-SWITCH vs Frequency

[1] If the bootrom or boot code generated by the tools accesses the switch, or if the user code needs access to SSCTRL, this low switch frequency must be factored into boot time and responsiveness expectations.

2.5 Busy Pipeline Power Consumption

Applications using four or more threads performing a significant amount of processing and which will not be spending much time waiting for events like low frequency port data input or timer timeouts, should add the IDD-DYN-BUSY component at the same frequency selected for IDD-DYN-BASE.

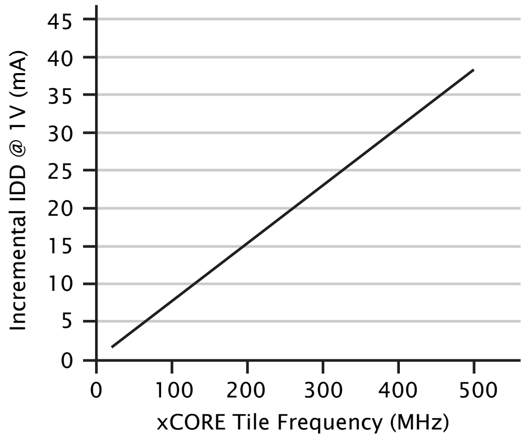

Figure 4: IDD-DYN-BUSY vs Frequency

2.6 Estimating Resource Related Power Consumption

The IDD-DYN-BASE component assumes the use of four ports and one timer. The IDD-DYN-RSRC component assumes use of up to 20 ports and four timers. Because applications can vary in their exact resource usage so widely, designers must place their application resource usage between these two points to decide whether to add in the IDD-DYN-RSRC component or some fraction of it.

Designers should bear in mind that applications making heavy use of port I/O or timers may well experience lower pipeline activity if many threads are paused waiting for events from ports or timers.

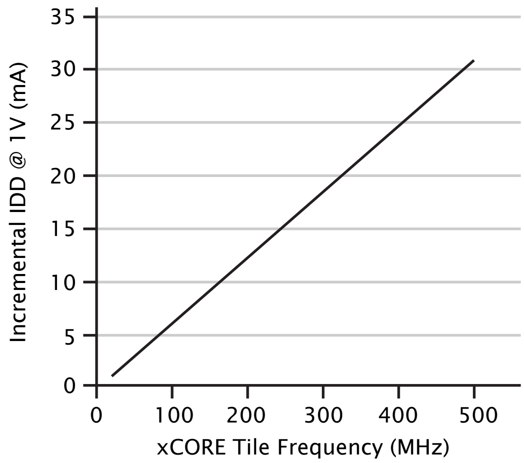

Figure 5: IDD-DYN-RSRC vs Frequency

3 Active Energy Conservation Mode

XS1 devices include an optional feature which will switch the xCORE frequency to its AEC setting when all active threads are paused waiting for input (for example, from a port or timer.

Normally the xCORE clock is supplied by a digital divider which selects an integer division (which can be 1) of the PLL output frequency. If AEC mode is enabled, the divider is switched to a second divider which is set to a higher division ratio in the event of all threads becoming paused. When any of the paused threads is woken due to the event it is waiting for completing, the xCORE clock is switched back to the main divider.

In general AEC mode will be suitable for sleep modes when an xCORE running at the lowered AEC frequency is able to detect the wake up event sufficiently quickly at the lowered AEC frequency that application timing constraints with respect to wake up are still met.

In this case the system power consumption should be divided between the mission mode and AEC frequencies according to an estimate of how much time will be spent in each mode.

This document uses IDD-DYN-BASE for AEC mode by looking up the lowered frequency from the IDD-DYN-BASE graph above. In practice, however, the actual current consumption in this mode is somewhat lower as there is no pipeline instruction processing activity at all when all threads are paused; the pipeline, however, is still be being clocked.

4 Estimating External Power Consumption

External power consumption (on the VDDIO supply) is dependent on the enabled peripherals in a given system. Each unique group of peripheral pins contributes to a piece of the overall external power, based upon several parameters:

- A — The number of output pins that switch during each cycle
- f — The maximum frequency at which the output pins can switch
- VDDIO — The voltage swing of the output pins
- C_L — The load capacitance of the output pins, including the capacitance of the pin itself[2].
- U — The utilization factor (the percentage of time that the peripheral is on and running) .

Use the above parameters to calculate the average external power (P_{EXT}) as follows:

$P_{EXT} = VDDIO^2 \times A \times C_L \times f \times U$

4.1 VDDIO

Please refer to the relevant device datasheet for VDDIO ranges and maximums.

4.2 General Purpose I/O

For general purpose I/O the system designer must determine the parameters A, f and U independently based on knowledge of the application.

4.3 XMOS Links

Where XMOS Links are used, the product of A x U x f can be replaced with the following equations:

2-wire mode: $AUF_{XMOS\ Link} = 10 \times simplex\_data\_rate_{link}$

5-wire mode: $AUF_{XMOS\ Link} = 4 \times simplex\_data\_rate_{link}$

Where $simplex\_data\_rate_{link}$ is the expected data rate of the link in megabytes/second. Note that this data rate should be the expected data rate of this particular link in this application context, which may be less than the maximum data rate the link is capable of. Also note that this parameter refers to the data rate in a single direction only. If bi-directional communication is taking place over a given XMOS Link, the power should be calculated once for each direction, using the appropriate data rates (which may not be symmetric).

4.4 Dedicated XMOS Links on XS1-L16 devices

If an XS1-L device is being used, there will likely be some communication between the two XS1 dies in the package, which may be conducted over up to four dedicated XMOS Links that connect the two dies in-package. In this case the power can be calculated as above, but using a value of 5pF for C_L, which is the load seen by an XMOS Link pin connected in-package on an XS1-L16 device.

[2] It is up to the user to determine the correct value of load capacitance C_L. This may not be an easy task since determining PCB trace capacitance is not straight forward. A network analyzer may be used where a Smith Chart is used to determine impedance of the trace. Extracting the capacitive element from the Smith Chart is the only component of the impedance that is needed for the equations. Alternatively, since PCBs are not yet manufactured early in the design process, the PCB layout engineers may be able to estimate capacitance of the trace based on line width, length, and board type. It is relatively easy to determine input capacitance of other devices on the PCB trace since these numbers are usually described in the respective datasheets. All of these capacitive elements must be summed and then added into the equation as the coefficient, C_L.}.

5 Thermal Limitations

For XS1-L processors, the total power budget is not limited by the maximum allowed junction temperature (TJ) of the device. For the L-series, even running all logic at the maximum frequency of 500 MHz, across the entire rated temperature range, there is no danger of getting close to a 125C junction temperature, even if the starting point is 85C ambient. All the XS1-L family packages have exposed die-paddles which improves thermal performance significantly.

Users should therefore consider the power budget purely in terms of their overall system since there are no package related constraints.

6 Conclusion

Several variables affect the power requirements of an embedded system. Measurements published in the XS1-L processor datasheets are indicative of typical parts running under typical conditions. However, these numbers do not reflect the actual numbers that may occur for a given processor under non-typical conditions. In addition to the type of silicon that the customer could have, the ambient temperature, core and system frequencies, supply voltages, pin capacitances, power modes, application code, and peripheral utilization contribute to the average total power that may be dissipated.

The average power estimates obtained from methods described in this document indicate how much the XS1-L processor loads a power source over time. These estimates are useful in terms of expected power dissipation within a system, but designs must support worst-case conditions under which the application can be run. Do not use this calculation to size the power supply, as the power supply must support peak requirements.

7 Examples

7.1 High Activity Single Chip Scenario, 500MHz

In this example a single XS1 device is running at its maximum rated frequency of 500MHz with 14 ports with a total of 26 I/O pins being used (some of them not fully utilized), for 40% of the time.

The remaining 60% of the time the XS1 is waiting for activity on input ports and uses the AEC feature to drop the xCORE clock frequency to 20MHz.

VDDIO is 3.3V .

The system is a single chip so the system switch is not needed. It is clocked at its maximum division ratio of 256 so IDD-DYN-SWITCH is not included.

The average power consumption of this system is therefore calculated at 106mA.

	500MHz mission mode	**20MHz AEC mode**
IDD-DYN-BASE	130 mA	4mA
IDD-DYN-STATIC	20 mA	20mA
IDD-DYN-BUSY	37 mA	0
0.5 x IDD-DYN-RSRC	15 mA	0
10 x 1-bit output ports at average switching frequency of 2MHz and C_L of 15pF with VDDIO=3.3V	10 x (15e-12) x 3.3^2 x 1e6 = 16.3 mA	0
2 x 8-bit ports at average switching frequency of 66MHz with 50% utilization and 5pF C_L with VDDIO=3.3V	16 x 0.5 x (5e-12) x 3.3^2 x 66e6 = 28mA	0
Totals	246mA	24mA
Scaled for utilization	40% (98.5 mA)	60% (14.4)
TOTAL	112.9 mA	

Table 2: Average Power for High Activity, Single Chip Scenario

7.2 Low Activity Two Chip, High I/O Count Scenario, 400MHz

In this example, there are two XS1 devices; device A boots from SPI Flash and then communicates with a slave device via 2 5-wire XMOS Links.

The slave device (chip A) has ten 1-bit output ports fully utilized at 2MHz. It does heavy processing work so the pipeline is assumed fully active and IDD-DYN-BUSY is included. It also uses a large number of input ports and timers so IDD-DYN-RSRC is included.

The master device (chip B) has one 16-bit port running at 20MHz. It switches its output pins 30% of the time with 15pF loads. The chip waits on data on an input port much of the time so IDD-DYN-BUSY is omitted for chip B. Likewise the total number of ports is small so IDD-DYN-RSRC is omitted for chip A. However chip A directs traffic at an estimated 22MBytes/sec per link, over two XMOS Links to chip A, so the power for two 5-wire XMOS Links operating at 22MBytes/sec is included. The traffic is almost all in the master-slave direction so link traffic returning in the other direction is ignored.

The average power consumption of this system is therefore calculated at 379mA.

	Chip A	**Chip B**
IDD-DYN-BASE	107 mA	214 mA
IDD-DYN-STATIC	20 mA	40 mA
IDD-DYN-BUSY (Chip A only)	30 mA	30 mA
1 x IDD-DYN-RSRC (chip A only)	30 mA	30 mA
1 x IDD-DYN-SWITCH (both chips @400MHz)	20 mA	40 mA
10 x 1-bit output ports at average switching frequency of 2MHz and C_L of 5pF with VDDIO=2.5V (chip A only)	10 pins x 5e-12 (C_L) x 2.5^2 x 2e6 = 0.6 mA	0.6 mA
1 x 16-bit port at average switching frequency of 20MHz with 30% utilization and 15pF C_L with VDDIO=2.5V (chip B only)	16 (pins) x 0.3 (%) x 15e-12 (C_L) x 2.5^2(VDDIO) x 20e6 (MHz) = 9mA	9 mA
2 x 5-wire mode XMOS Links T_{symbol}=7.5ns, C_L= 15pF, operating at 22Mbytes/sec, VDDIO=2.5V, simplex only	4 (5w mode) x 22e6 (Mbtye/sec) x 2.5^2 (VDDIO) x 2 (links) x 15e-12 (C_L)	16.4mA
Totals	246mA	379 mA

Table 3: Average Power for Low Activity, High I/O Count, Multiple Chip Scenario